CC Technical Documentation
RM-11 Series Transceivers

Troubleshooting - Baseband

Issue 2 09/2005

Contents

Page

This page intentionally left blank.

Introduction

The baseband module is a trimode CDMA dual-band engine based on the DCT4 architecture. The baseband consists of three main ASIC's:

- Universal Energy Management (UEM)
- Universal Phone Processor (UPP)
- 128-Megabit flash

The baseband architecture supports a power-saving function called "sleep mode". Sleep mode shuts off the VCTCXO, which is used as system clock source for both RF and baseband. During the sleep mode, the system runs from a 32 kHz crystal. The mobile terminal awakes by a timer running from this 32 kHz clock. The sleep time is determined by network parameters. Sleep mode is entered when both the MCU and the DSP are in standby mode and the 19.2 MHz Clk (VCTCXO) is switched off.

The mobile terminal supports both two and three DCT3 type wire chargers. However, the three-wire chargers are treated as two-type wire chargers. Charging is controlled by UEM ASIC and EM SW.

BLD-3 Li-ion battery is used as main power source and has a nominal capacity of 780 mAh.

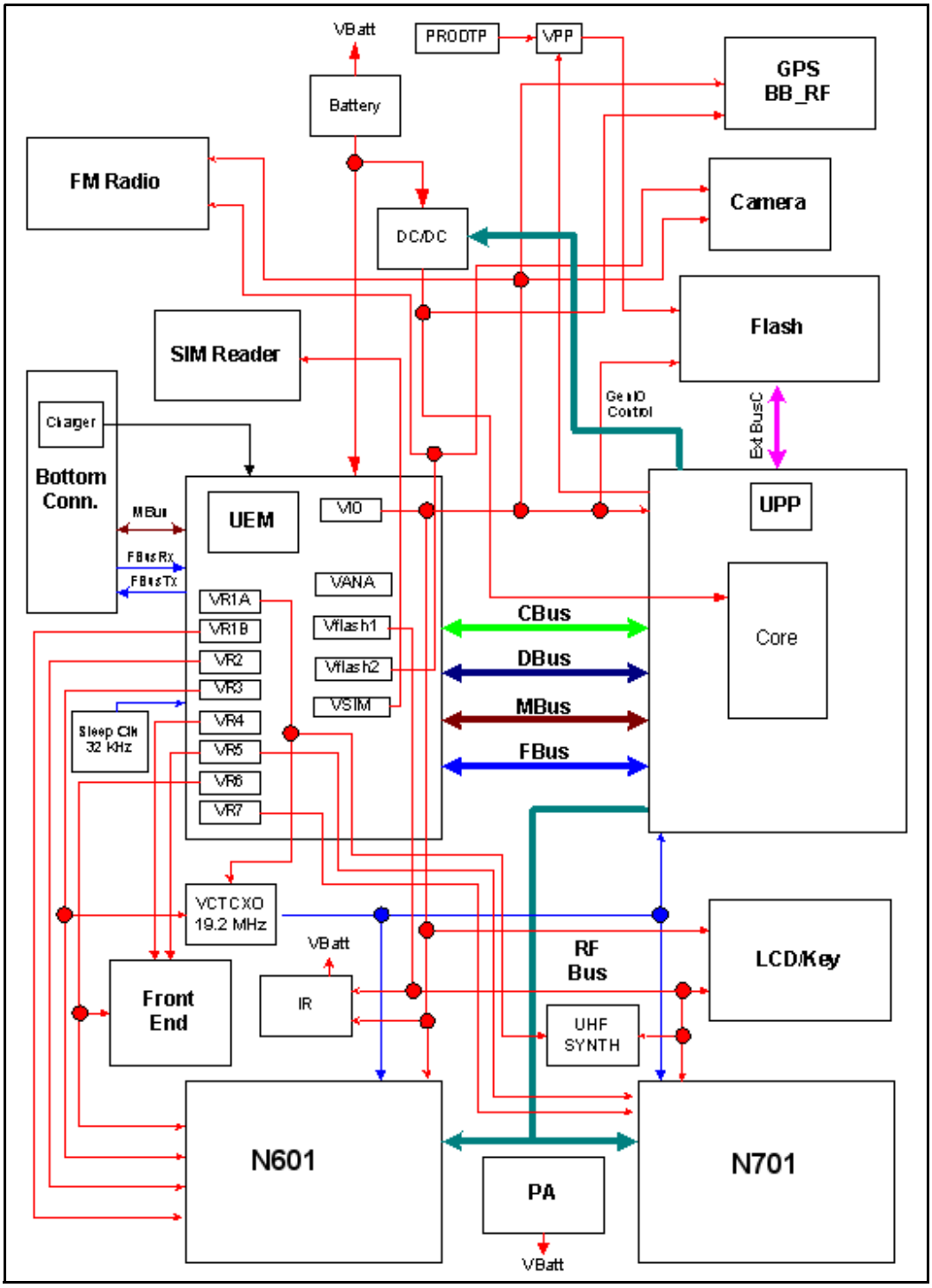


Figure 1: Power distribution

Power Up and Reset

Power up and reset is controlled by the UEM ASIC. The baseband can be powered up in the following ways:

- By the Power button, which means grounding the PWRONX pin of the UEM
- By connecting the charger to the charger input
- By the RTC Alarm, when the RTC logic has been programmed to give an alarm

After receiving one of the above signals, the UEM counts a 20 ms delay and then enters reset mode. The watchdog starts, and if the battery voltage is greater than Vcoff+, a 200 ms delay is started to allow references to settle. After this delay elapses, the VFLASH1 regulator is enabled. Then, 500 us later VR3, VANA, VIO, and VCORE are enabled. Finally, the PURX (Power Up Reset) line is held low for 20 ms. This reset, PURX, is fed to the baseband ASIC UPP; resets are generated for the MCU and the DSP. During this reset phase, the UEM forces the VCTCXO regulator on — regardless of the status of the sleep control input signal — to the UEM. The FLSRSTx from the ASIC is used to reset the flash during power up and to put the flash in power down during sleep. All baseband regulators are switched on when the UEM powers on. The UEM internal watchdogs are running during the UEM reset state, with the longest watchdog time selected. If the watchdog expires, the UEM returns to power-off state. The UEM watchdogs are internally acknowledged at the rising edge of the PURX signal in order to always give the same watchdog response time to the MCU.

The following diagram represents UEM start-up sequence from reset to power-on mode.

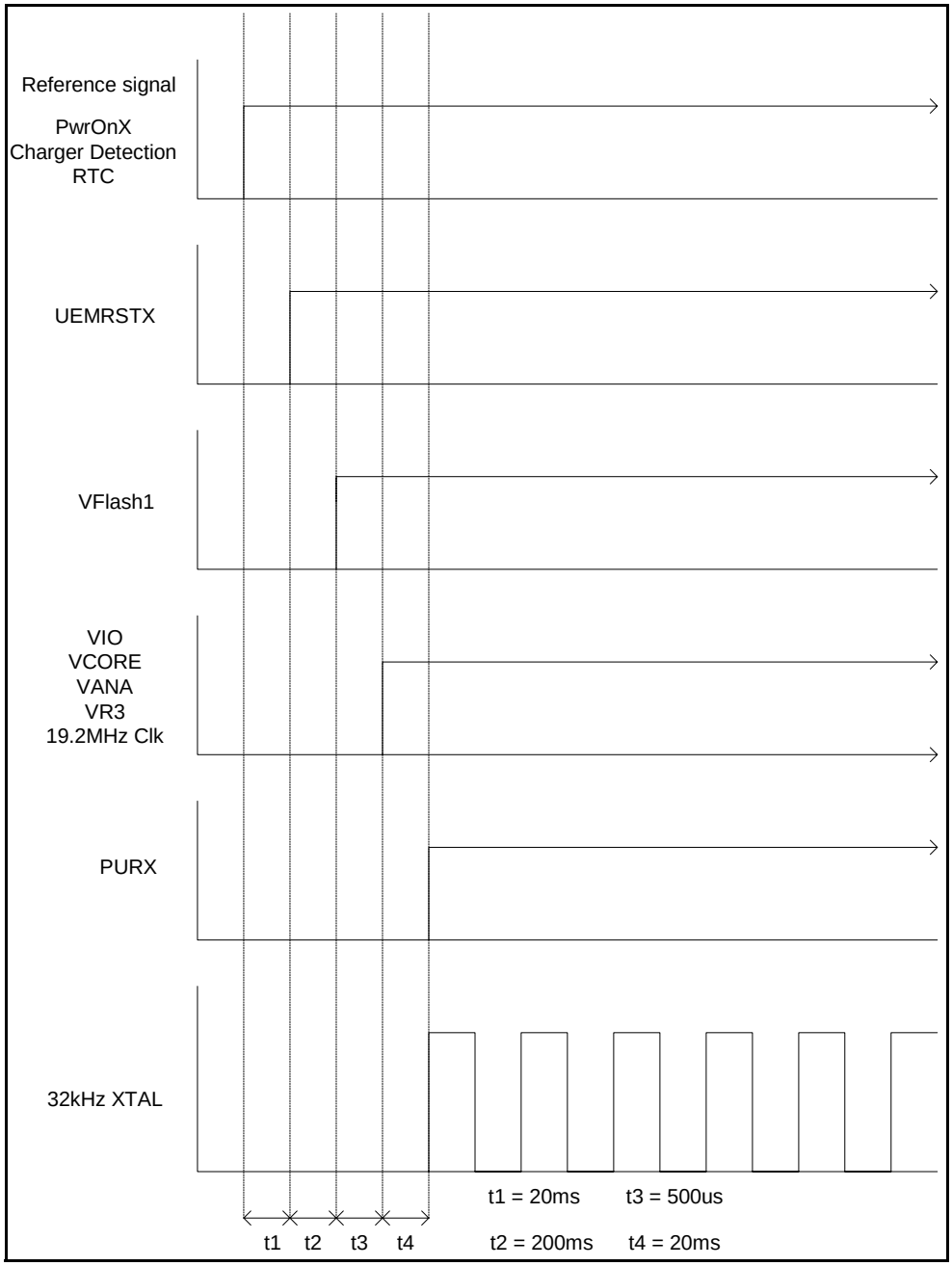
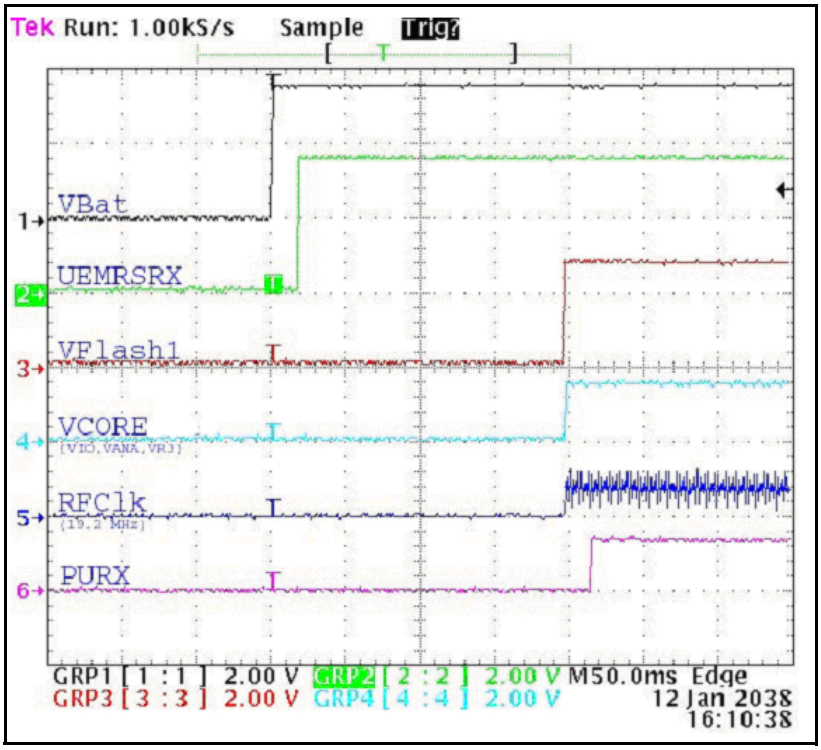


Figure 2: Power-up timing sequence


Tek Run: 1.00kS/s Sample Trig?
VBat
UEMRSRX
VFlash1
VCORE
RFClk
PURX
GRP1 [1 : 1] 2.00 V GRP2 [2 : 2] 2.00 V M50.0ms Edge
GRP3 [3 : 3] 2.00 V GRP4 [4 : 4] 2.00 V 12 Jan 2038
16:10:38

Power Key

When the power on key is pressed, the UEM enters the power up sequence. Pressing the power key causes the PWRONX pin on the UEM to be grounded. The UEM PWRONX signal is not part of the keypad matrix. The power key is only connected to the UEM. This means that when pressing the power key, an interrupt is generated to the UPP that starts the MCU. The MCU then reads the UEM interrupt register and notices that it is a PWRONX interrupt. The MCU now reads the status of the PWRONX signal using the UEM control bus, CBUS. If the PWRONX signal stays low for a certain time, the MCU accepts this as a valid power on state and continues with the SW initialization of the baseband. If the power on key does not indicate a valid power on situation the MCU powers off the baseband.

Charger is Connected

In order to be able to detect and start charging in the case where the main battery is fully discharged (empty) and hence UEM has no supply (NO_SUPPLY or BACKUP mode of UEM), charging is controlled by start-up charging circuitry.

Whenever the VBAT level is detected to be below the master reset threshold (VMSTR-), charging starts and is controlled by the start-up charge circuitry. Connecting a charger forces the VCHAR input to rise above the charger detection threshold (VCHDET+) and by detection charging is started. The UEM generates a 100mA constant output current from the connected charger's output voltage. As the battery charges, its voltage rises and when VBAT voltage level is detected to be higher than the master reset threshold limit (VMSTR+), the start-up charge is terminated.

Monitoring the VBAT voltage level is done by the charge control block (CHACON). MSTRX='1' output reset signal (internal to the UEM) is given to the UEM's RESET block when VBAT>VMSTR+ and UEM enters into reset sequence.

If VBAT is detected to fall below VMSTR- during start-up charging, charging is cancelled. It restarts if a new rising edge on VCHAR input is detected (VCHAR rising above VCHDET+).

RTC Alarm

If the mobile terminal is in power off mode when the RTC alarm occurs, a wake-up procedure initiates. After the baseband is powered on, an interrupt is given to the MCU. When the RTC alarm occurs during active mode, an interrupt to the MCU is generated.

Power Off

The baseband switches into power off mode if any of following statements is true:

- Power key is pressed
- Battery voltage is too low (VBATT < 3.2 V)
- Or if Watchdog timer register expires

The power down procedure is controlled by the UEM.

Power Consumption and Operation Modes

During power off mode, power (VBAT) is supplied to UEM, buzzer, vibra, LED, PA and PA drivers (N603 and N602). During this mode, the current consumption on this mode is approximately 35 uA. This is the UEM leakage current.

In sleep mode, both processors, MCU and DSP, are in stand-by mode. The mobile terminal will go to sleep mode only when by both processors made this request. When SLEEPX signal is detected low by the UEM, the mobile terminal enters SLEEP mode. VIO and VFLASH1 regulators are put into low quiescent current mode, VCORE enters LDO mode and VANA and VFLASH2 regulators are disabled. All RF regulators are disabled during SLEEP mode. When SLEEPX signal is detected high by the UEM, the mobile terminal enters ACTIVE mode and all functions are activated.

The sleep mode is exited either by the expiration of a sleep clock counter in the UEM or by some external interrupt, generated by a charger connection, key press, headset connection etc.

In sleep mode, the VCTCXO (19.2 MHz Clk) is shut down and the 32 kHz sleep clock oscillator is used as reference clock for the baseband.

The average current consumption of the mobile terminal can vary depending mainly on the software state (e.g., slot cycle 0, 1, 2) and if the mobile terminal is working on IS95 or IS2000 for CDMA. However, on average it is about 6 mA in slot cycle 0 on IS95.

In the Active mode, the mobile terminal is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. There are several sub-states in the active mode depending on the mobile terminal present state such as: burst reception, burst transmission, if DSP is working etc.

In active mode, software controls the UEM RF regulators VR1A and VR1B, which can be enabled or disabled. These regulators work with the UEM charge pump. VSIM can be enabled or disabled and its output voltage can be programmed at 1.8 V or 3.3 V. VR2 and VR4—VR7 can be enabled or disabled or forced into low quiescent current mode. VR3 is always enabled in active mode and disabled during sleep mode and cannot be controlled by software in the same way as the other regulators. VR3 only turns off if both processors (DSP and MCU) request to be in sleep mode.

Charging mode can be performed in parallel with any other operating mode. A BSI resistor inside the battery indicates the battery type/size. The resistor value corresponds to a specific battery type and capacity. This capacity value is related to the battery technology.

The battery voltage, temperature, size and charging current are measured by the UEM, and the EM charging algorithm controls it.

The charging control circuitry (CHACON) inside the UEM controls the charging current delivered from the charger to the battery. The battery voltage rise is limited by turning the UEM switch off when the battery voltage has reached 4.2 V. Charging current is monitored by measuring the voltage drop across a 220 mOhm resistor.

Power

In normal operation, the baseband is powered from the mobile terminal's battery. The battery consists of one Lithium-Ion cell with a capacity of 780 mAh.

The UEM ASIC controls the power distribution to whole mobile terminal through the BB and RF regulators excluding the power amplifier (PA) and the DC/DC, which have a continuous power rail directly from the battery. The battery feeds power directly to the following parts of the system:

- UEM
- PA
- DC/DC
- Buzzer
- Vibra
- Display and keyboard lights

The heart of the power distribution to the mobile terminal is the UEM. It includes all the voltage regulators and feeds power to the whole system. The UEM handles hardware functions of power up so that regulators are not powered and power up reset (PURX) is not released if the battery voltage is less than 2.8 V.

The baseband is powered from five different UEM regulators:

Table 1: Baseband Regulators

Regulator	Maximum Current (mA)	Vout (V)	Notes
VCORE DC/DC	300	1.5	Output voltage selectable 1.0V/1.3V/1.5V/1.8V Default power at power-up is 1.5V
VIO	150	1.8	Enabled always except during power-off mode
VFLASH1	70	2.78	Enabled always except during power-off mode

Table 1: Baseband Regulators (Continued)

Regulator	Maximum Current (mA)	Vout (V)	Notes
VFLASH2	40	2.78	Enabled only when data cable is connected
VANA	80	2.78	Enabled only when the system is awake (off during sleep and power-off modes)
VSIM	25	3.0	Enabled during power-up mode and scanning for a SIM card

Table 2 includes the UEM RF regulators.

Table 2: RF Regulators

Regulator	Maximum Current (mA)	Vout (V)	Notes
VR1A	10	4.75	Enabled when cell receiver is on
VR1B	10	4.75	Enabled when the transmitter is on
VR2	100	2.78	Enabled when the transmitter is on
VR3	20	2.78	Enabled when SleepX is high
VR4	50	2.78	Enabled when the receiver is on
VR5	50	2.78	Enabled when the receiver is on
VR6	50	2.78	Enabled when the transmitter is on
VR7	45	2.78	Enabled when the receiver is on

A charge pump used by VR1A is constructed around UEM. The charge pump works with Cbus (1.2 MHz Clk) and gives a 4.75 V regulated output voltage to RF.

Clock Distribution

RFClk (19.2 MHz Analog)

The main clock signal for the baseband is generated from the voltage and temperature controlled crystal oscillator (VCTCXO), G503. This 19.2 MHz clock signal is generated at the RF and fed to RFCLK pin of the UPP.

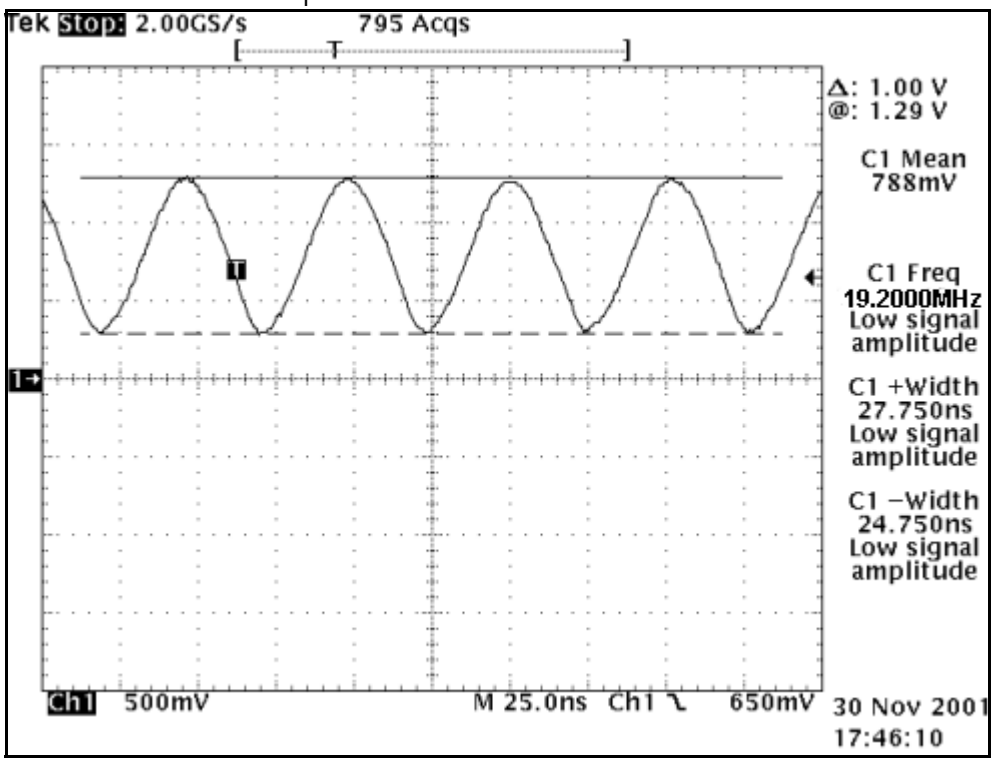


Figure 3: Waveform of the 19.2MHz clock (VCTCXO)

RFConvClk (19.2 MHz digital)

The UPP distributes the 19.2 MHz Clk to the internal processors, the DSP, and MCU, where the software multiplies this clock by seven for the DSP and by two for the MCU.

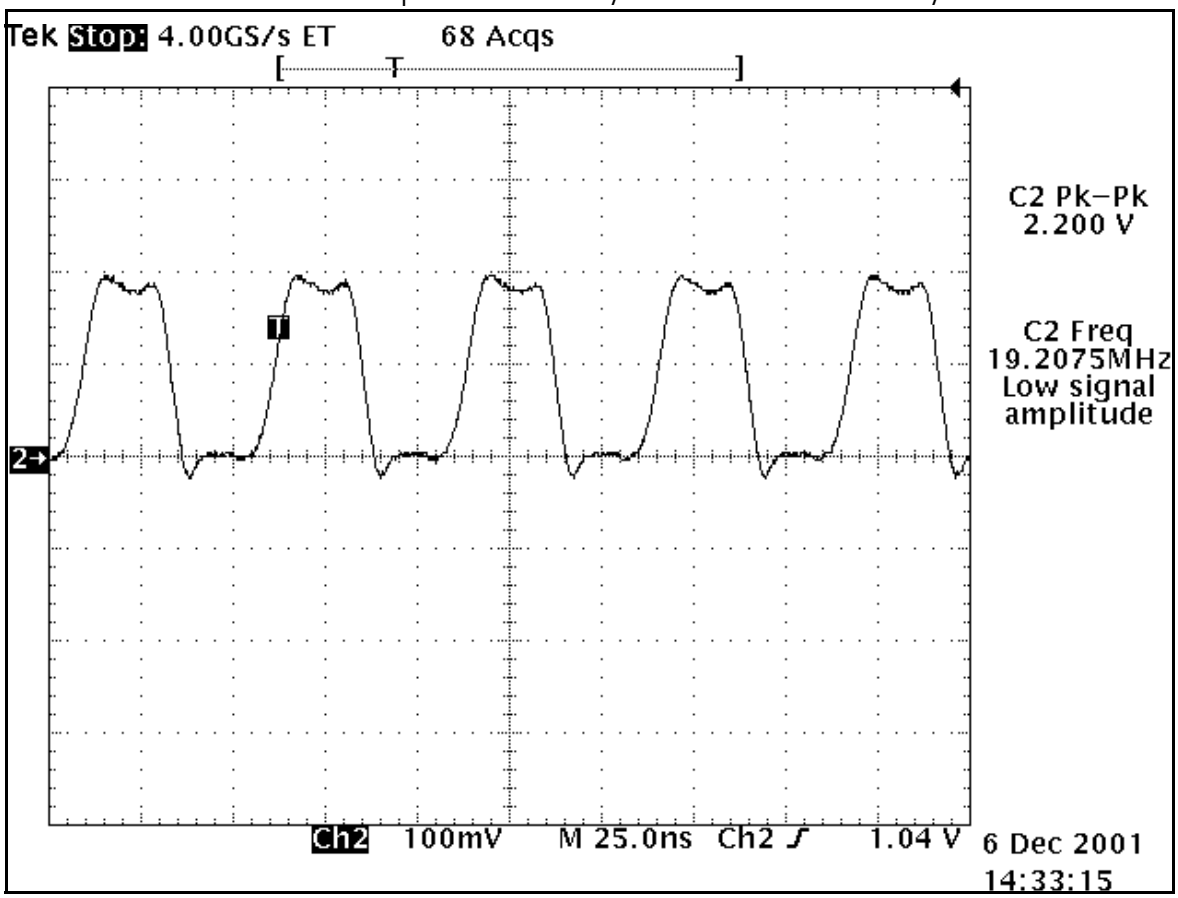


Figure 4: RFCovCLk waveform

CBUSClk Interface

A 1.2 MHz clock signal is used for CBUS, which is used by the MCU to transfer data between the UEM and UPP.

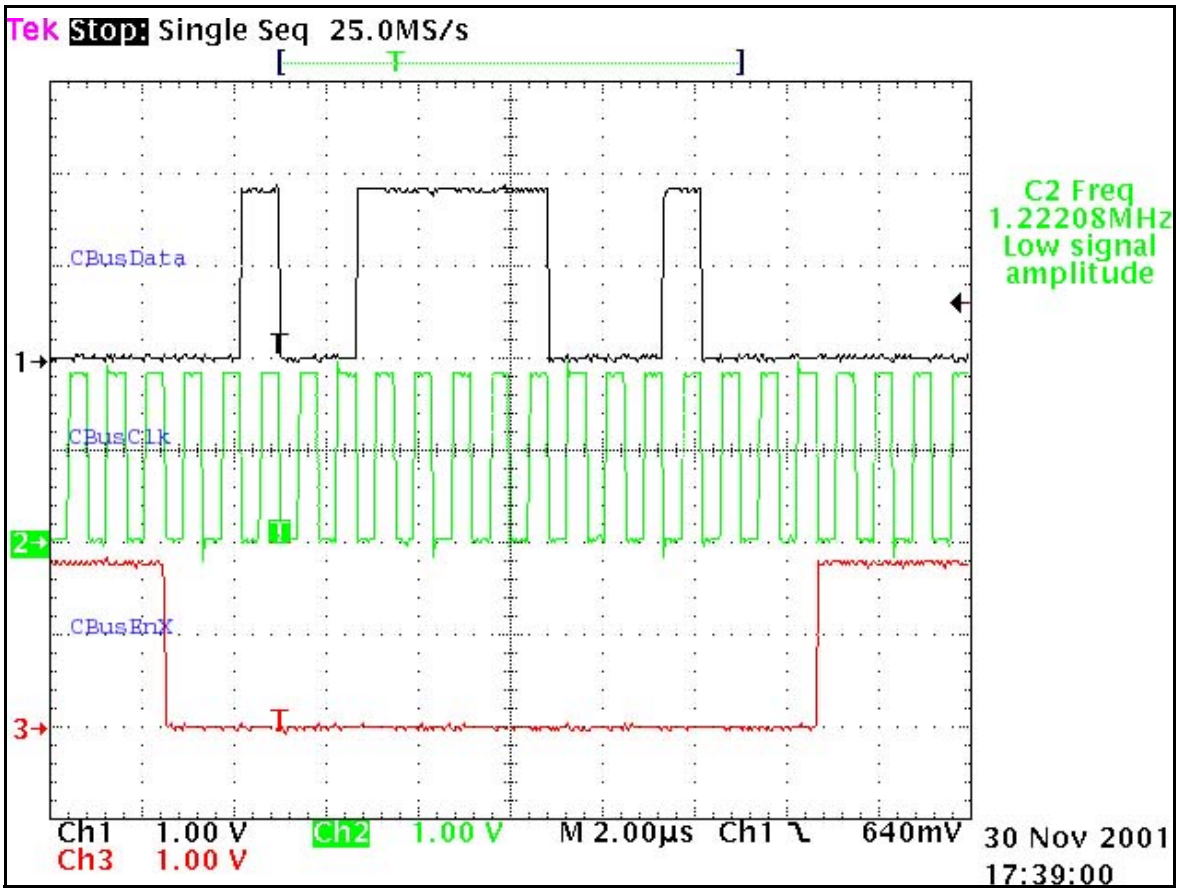


Figure 5: CBUS data transfer

DBUS Clk Interface

A 9.6 MHz clock signal is used for DBUS, which is used by the DSP to transfer data between the UEM and UPP.

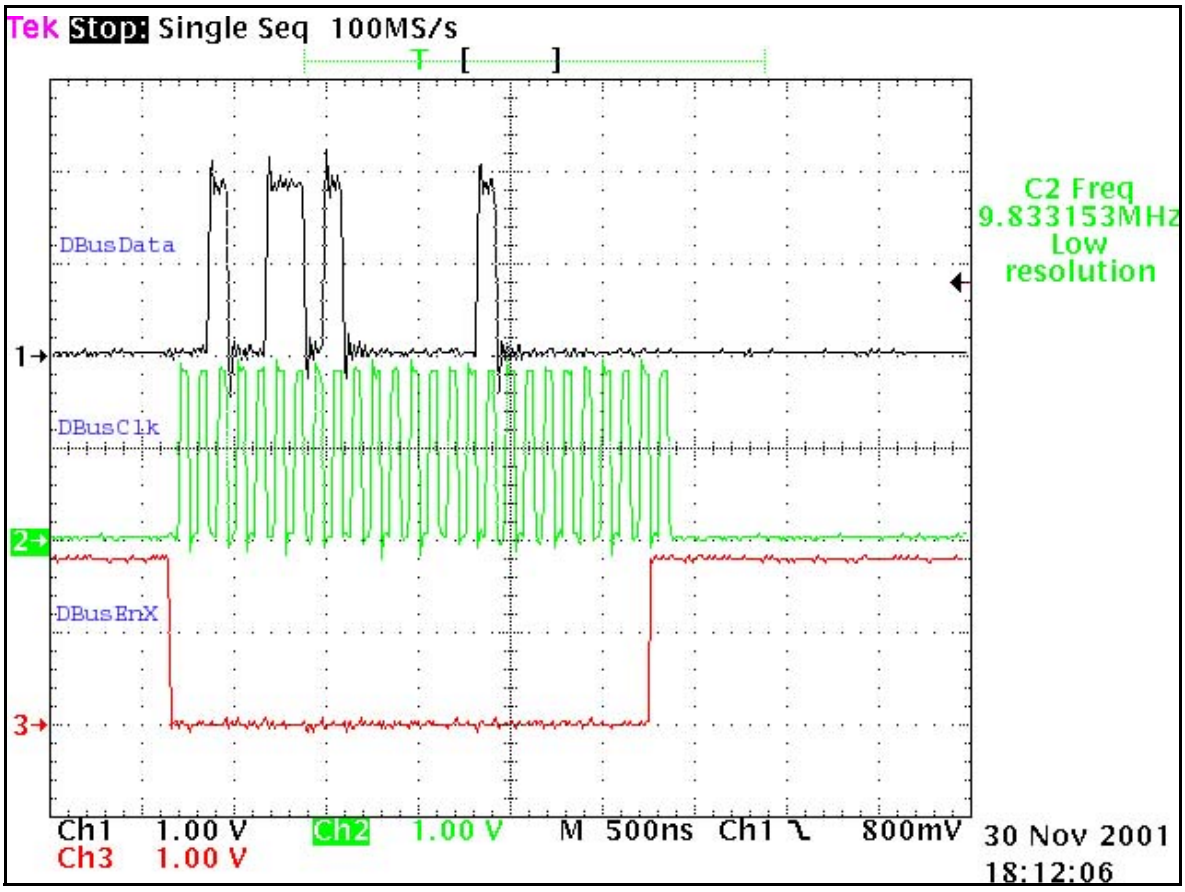


Figure 6: DBUS data transfer

The system clock can be stopped during sleep mode by disabling the VCTCXO power supply from the UEM regulator output (VR3) and turning off the controlled output signal SleepX from the UPP.

SleepCLK (Digital)

The UEM provides a 32 kHz sleep clock for internal use and to the UPP, where it is used for the sleep mode timing.

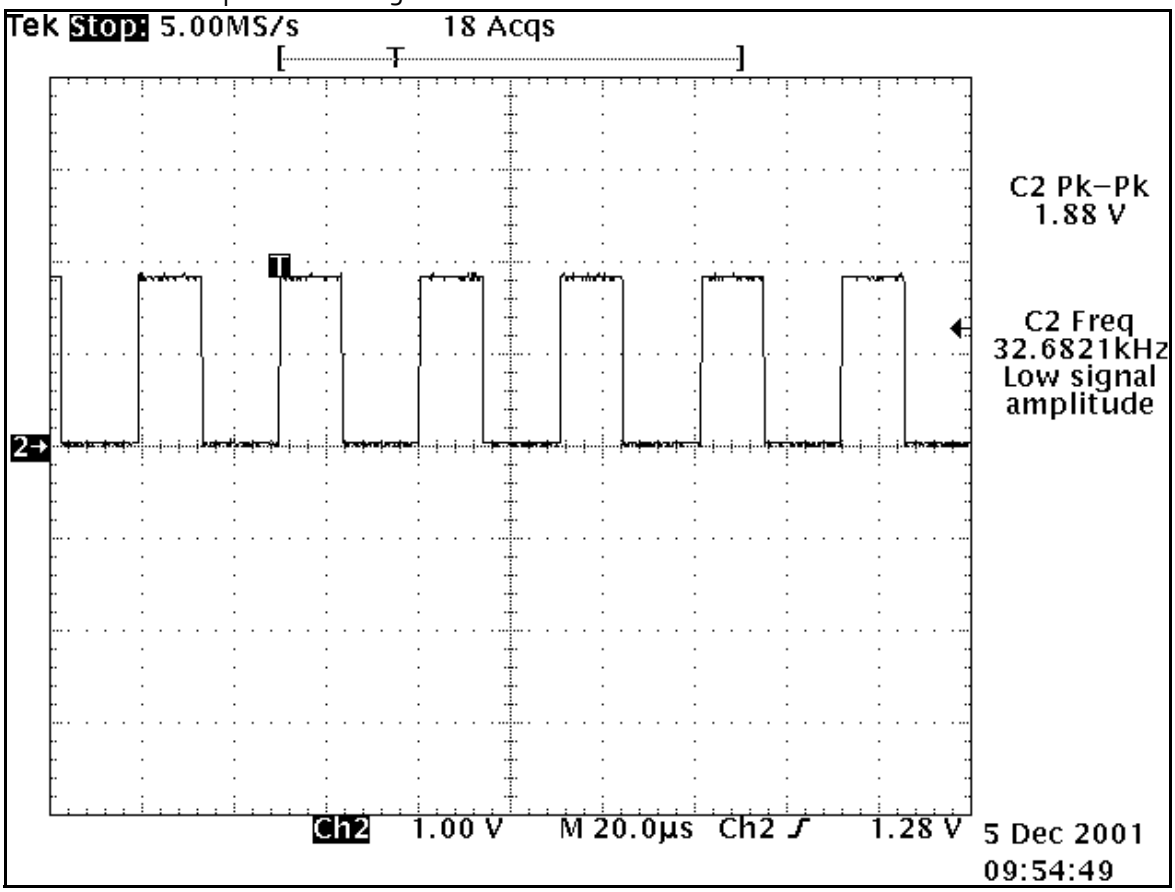


Figure 7: 32 kHz Digital output from UEM

SleepCLK (Analog)

When the system enters sleep mode or power off mode, the external 32 KHz crystal provides a reference to the UEM RTC circuit to turn on the mobile terminal during power off or sleep mode.

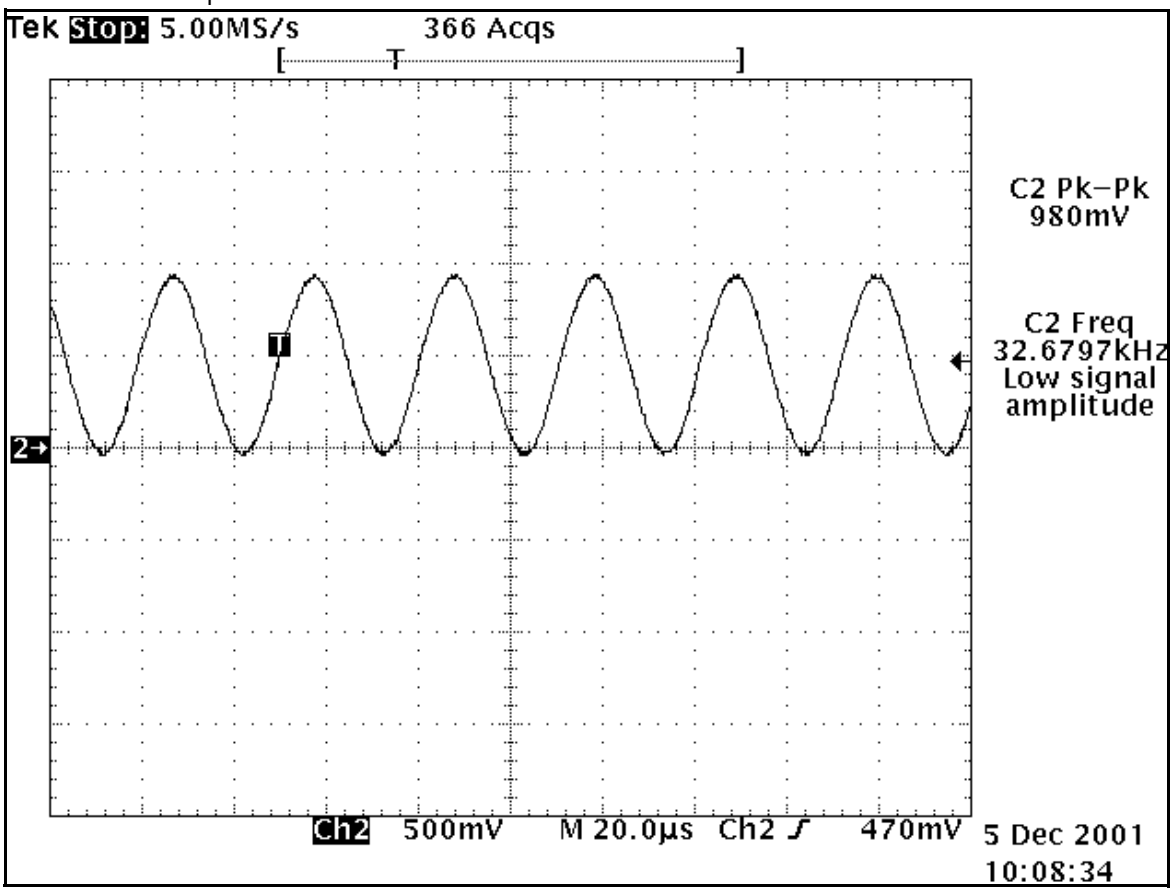


Figure 8: 32 KHz analog waveform at 32 KHz crystal input

Flash Programming Error Codes

The following characteristics apply to the information in Table 3.

- Error codes can be seen from the test results or from Phoenix's flash-tool.
- Underlined information means that the connection under consideration is being used for the first time.

Table 3: Flash Programming Error Codes

Error	Description	Not Working Properly
C101	"The Phone does not set FbusTx line high after the startup."	Vflash1 VBatt BSI and FbusRX from prommer to UEMC. FbusTx from UPP->UEMC->Prommer(SA0)
C102	"The Phone does not set FbusTx line low after the line has been high. The Prommer generates this error also when the Phone is not connected to the Prommer."	PURX(also to Safari) VR3 Rfclock(VCTCXO->Safari->UPP) Mbus from Prommer->UEMC->UPP(MbusRx)(SA0) FbusTx from UPP->UEMC->Prommer(SA1) BSI and FbusRX from prommer to UEMC.
C103	" Boot serial line fail."	Mbus from Prommer->UEMC->UPP(MbusRx)(SA1) FbusRx from Prommer->UEMC->UPP FbusTx from UPP->UEMC->Prommer
C104	"MCU ID message sending failed in the Phone."	FbusTx from UPP->UEMC->Prommer
C105	"The Phone has not received Secondary boot codes length bytes correctly."	Mbus from Prommer->UEMC->UPP(MbusRx) FbusRx from Prommer->UEMC->UPP FbusTx from UPP->UEMC->Prommer
C106	"The Phone has not received Secondary code bytes correctly."	Mbus from Prommer->UEMC->UPP(MbusRx) FbusRx from Prommer->UEMC->UPP FbusTx from UPP->UEMC->Prommer
C107	"The Phone MCU can not start Secondary code correctly."	UPP
C586	"The erasing status response from the Phone informs about fail."	Flash
C686	"The programming status response from the Phone informs about fail."	Flash
Cx81	"The Prommer has detected a checksum error in the message, which it has received from the Phone."	FbusTx from UPP->UEMC->Prommer
Cx82	"The Prommer has detected a wrong ID byte in the message, which it has received from the Phone."	FbusTx from UPP->UEMC->Prommer

Table 3: Flash Programming Error Codes (Continued)

Error	Description	Not Working Properly
A204 Cx83 Cx84 Cx85	"The flash manufacturer and device IDs in the existing algorithm files do not match with the IDs received from the target phone." "The Prommer has not received phone acknowledge to the message." "The phone has generated NAK signal during data block transfer." "Data block handling timeout"	Flash UPP VIO/VANA Signals between UPP-Flash Mbus from Prommer->UEMC->UPP(MbusRx) FbusRx from Prommer->UEMC->UPP FbusTx from UPP->UEMC->Prommer
Cx87	"Wrong MCU ID."	RFClock UPP(Vcore)
Startup for flashing	Required startup for flashing	Vflash1 VBatt

Charging Operation

Battery

A Lithium-Ion cell battery with a capacity of 780 mAh is used. Reading a resistor inside the battery pack on the BSI line indicates the battery size. NTC-resistor inside the battery measures the battery temperature on the BTEMP line.

Temperature and capacity information are needed for charge control. These resistors are connected to BSI and BTEMP pins of battery connector. The mobile terminal has 100 kW pull-up resistors for these lines so that they can be read by A/D inputs in the mobile terminal.

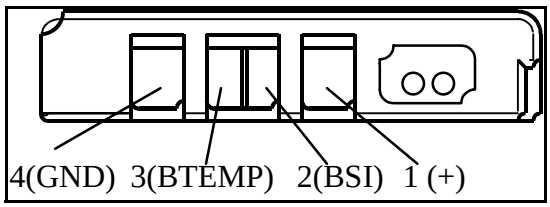


Figure 9: BLD-3 battery pack pin order

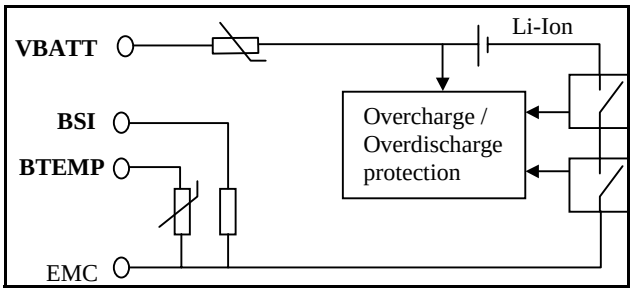


Figure 10: Interconnection diagram inside the battery pack

Charging Circuitry

The UEM controls charging depending on the charger being used and the battery size. External components are needed for EMC, reverse polarity and transient protection of the input to the baseband module. The charger connection is through the system connector interface. The baseband is designed to support DCT3 chargers from an electrical point of view. Both 2- and 3-wire type chargers are supported. However, as mention above, three wire chargers are treated as two.

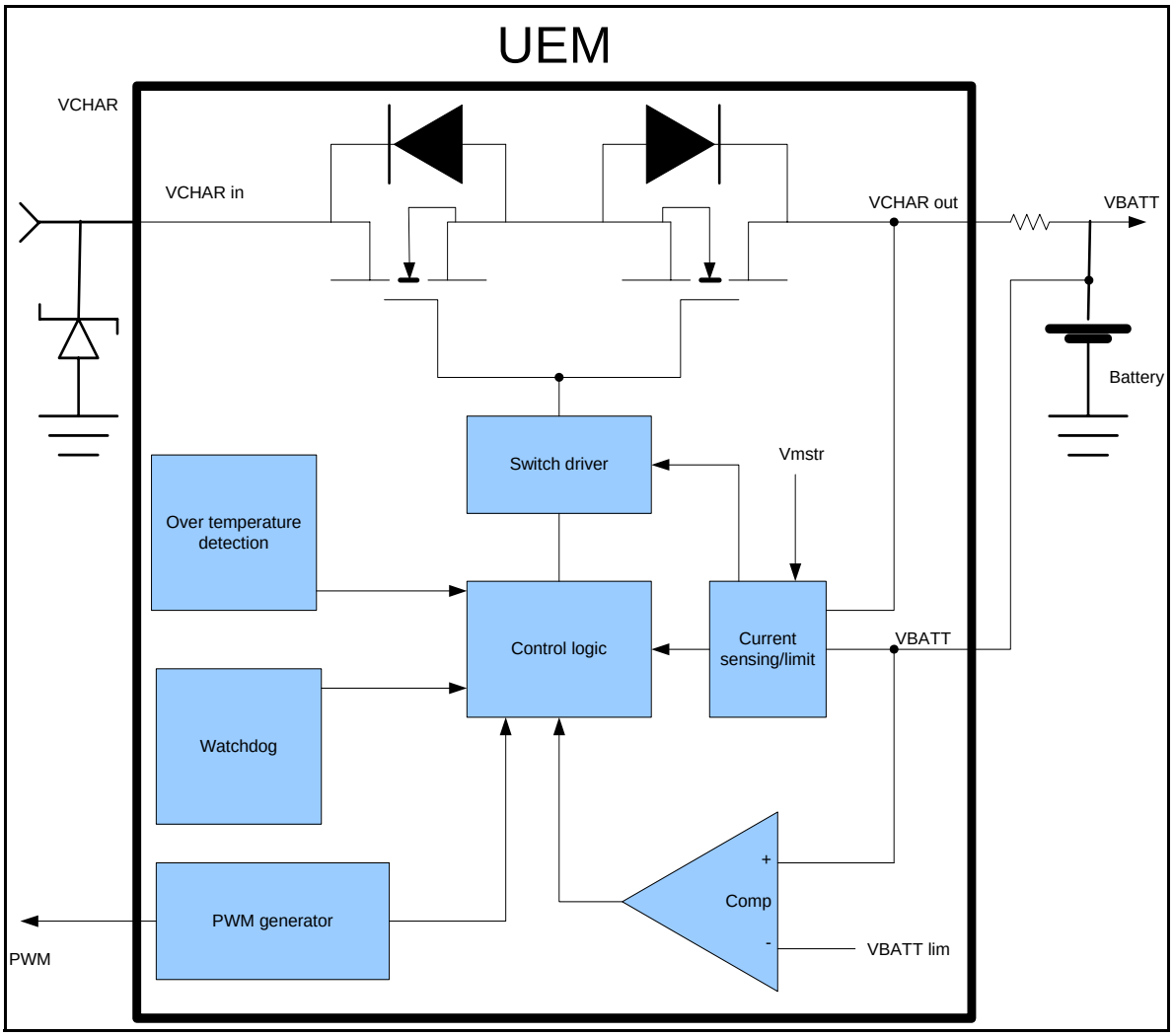


Figure 11: Charging circuitry

Charger Detection

Connecting a charger creates voltage on VCHAR input of the UEM. When VCHAR input voltage level is detected to rise above 2 V (VCHdet+ threshold) by UEM charging starts. VCHARDET signal is generated to indicate the presence of the charger for the software. The charger identification/acceptance is controlled by EM software.

The charger recognition is initiated when the EM software receives a "charger connected" interrupt. The algorithm basically consists of the following three steps:

1. Check that the charger output (voltage and current) is within safety limits.
2. Identify the charger as a two-wire or three-wire charger.
3. Check that the charger is within the charger window (voltage and current).

If the charger is accepted and identified, the appropriate charging algorithm is initiated.

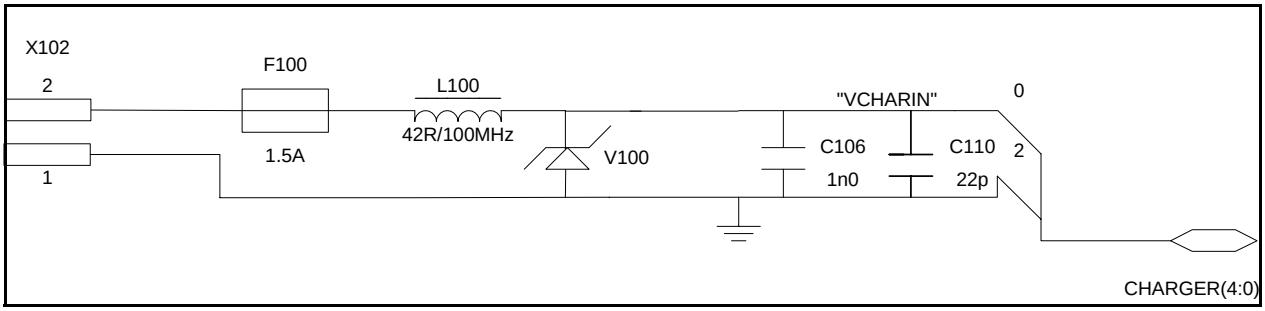


Figure 12: Charging circuit

Charge Control

In active mode, charging is controlled by the UEM's digital part. Charging voltage and current monitoring is used to limit charging into a safe area. For that reason, the UEM has programmable charging cut-off limits:

- VBATLim1=3.6 V (Default)
- VBATLim2L=5.0 V and
- VBATLim2H=5.25 V.

VBATLim1, 2L, 2H are designed with hystereses. When the voltage rises above VBATLim1, 2L, 2H+ charging is stopped by turning the charge switch off. There are no changes to the operational mode. After voltage has decreased below VBATLim-, charging re-starts.

There are two PWM frequencies in use depending on the type of the charger: the 2-wire charger uses a 1 Hz and a 3-wire charger uses a 32 Hz. The duty cycle range is 0% to

100%. The maximum charging current is limited to 1.2 A.

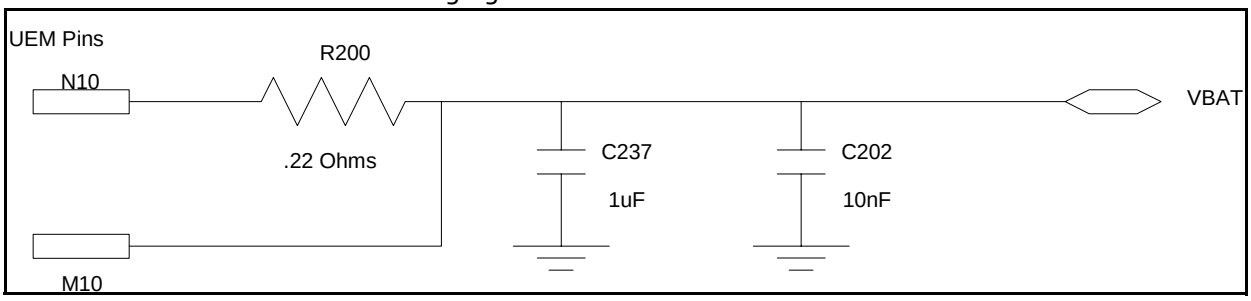


Figure 13: Charging circuit at battery

Audio

The audio control and processing is supported by the UEM, which contains the audio codec, and by the UPP, which contains the MCU and DSP blocks that handle and process the audio data signals.

The baseband supports three microphone inputs and two earpiece outputs. The microphone inputs are MIC1, MIC2, and MIC3. MIC1 input is used for the mobile terminal's internal microphone; MIC2 is used for headsets (HDB-4). MIC3 is used for the Universal Headset. Every microphone input can have either a differential or a single-ended AC connection to the UEM circuit. The internal microphone MIC1 and external microphone MIC2 for Pop-port™ accessory detection are both differential. However, the Universal Headset interface is single-ended. The microphone signals from different sources are connected to separate inputs at the UEM. Inputs for the microphone signals are differential. Also, the MICB1 is used for MIC1 and the MICB2 is used for MIC2 and MIC3 (Universal Headset).

Display and Keyboard

There are three LEDs for the LCD and eight LEDs for the keypad. The KLIGHT signal is used to drive the LED driver for the LCD and keyboard. The color LCD uses 9-bit data transfer. The interface is quite similar to DCT3-type interface, except Command/Data information is transferred together with the data. The D/C bit is set during each transmitted byte.

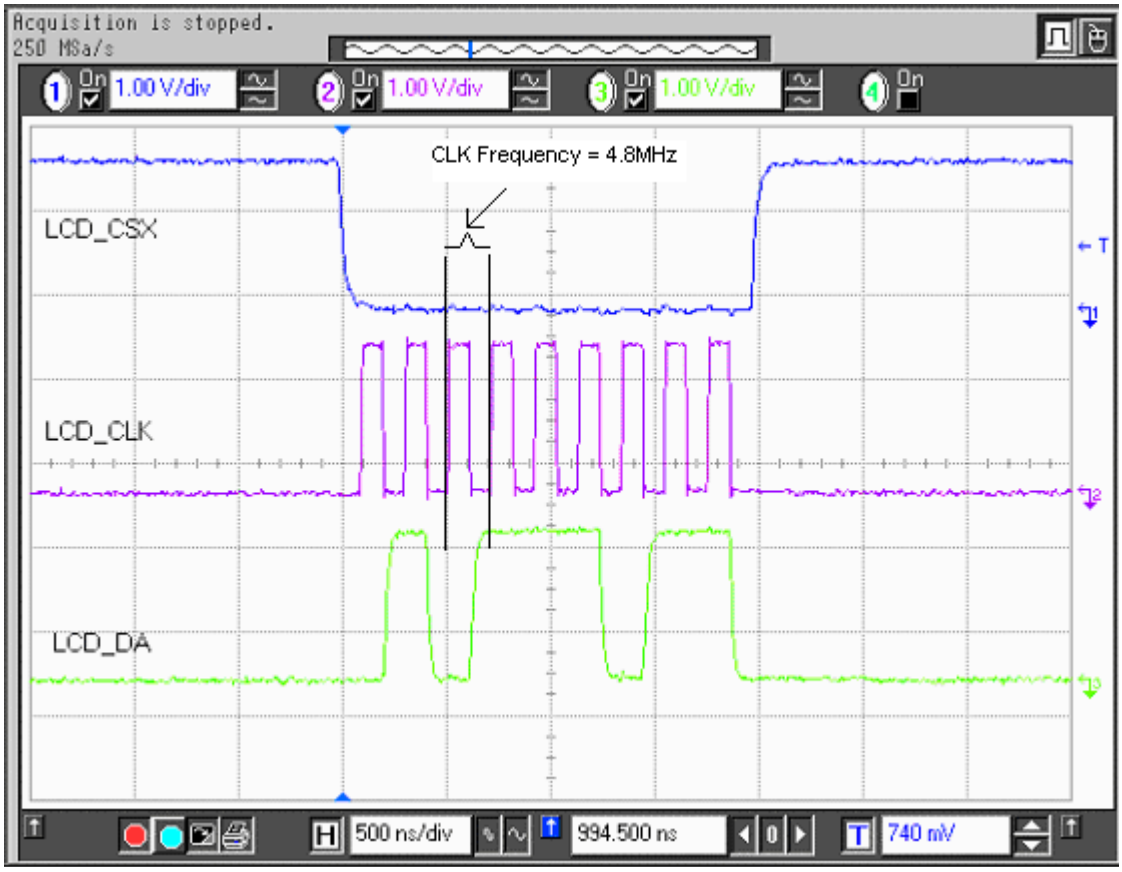


Figure 14: CLK frequency

FM Radio

FM radio circuitry is implemented using highly integrated radio IC (TEA5767HN) and is controlled by the MCU software through a serial bus (GenIOS) interface.

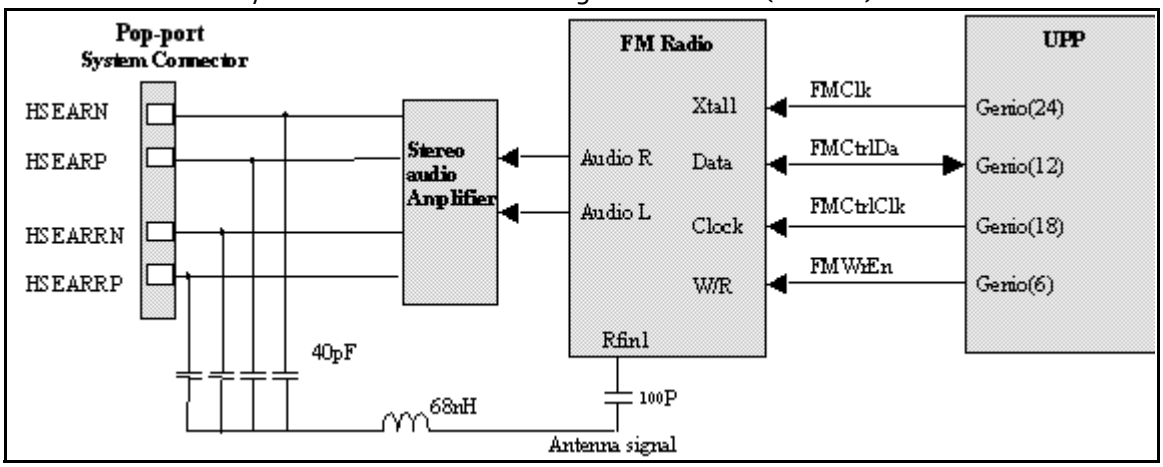


Figure 15: FM Radio (N356) audio (N150), antenna, and digital interface connections

Table 4: FM Radio Interface Timing

FM Radio Signal	Min	Max	Condition	Note
FMWrEn	20µs		t_{wd}	FMWrEn high before rising edge of FMCtrlClk (write operation)
FMCtrlClk	50ms	1 µs	t_r/t_f t_{start}	rise/fall time FMCtrlClk delay after switching on the VFLASH2
FMCtrlDa	10 µs 1.5 µs 20 µs	14 µs	t_{da} t_{shift} t_{hold} t_{setup}	Shift register available after "search ready" Data available after FMCtrlClk rising edge (read operation) FMCtrlDa stable after FMCtrlClk rising edge (write operation) FMCtrlDa set before FMCtrlClk rising edge (write operation)

While write/read is high, the microcontroller can transmit data to the TEA5767. At the rising edge of the bus clock, the register shifts and accepts the stable bit. At clock low the microcontroller writes the following bit. A tuning function starts when the write/ read signal changes from high to low. If a search tuning request is sent, the IC autonomously starts searching the FM band. The search direction and search stop level can be chosen. If a station with a field strength equal to or higher than this stop level is found, the tuning system stops and the Found Flag bit is set to high. If a band limit is reached during the search, the tuning system stops at the band limit, the Band Limit flag bit is set to high, and the Found Flag is set to high.

While write/read is low, data can be read by the UPP. At the rising edge of the BUS Clock, data is shifted out of the register. This data is available from the point where the bus clock is high until the next rising edge of the clock occurs.

The stereo audio output signals are fed to the stereo amplifier. Volume control of the FM audio signal is made by circuitry inside the amplifier. The amplified audio signal is fed to the headset or IHF speaker. The headset is also used as the antenna input for the radio.

FM Radio Test

To hear the FM radio, you first connect the headset to the Pop-port™ or UHJ ports because the headset is an FM radio antenna. Connect the headset to the UHJ port to control the FM radio by using Phoenix. If you connect a headset (such as an HDS-3) to the Pop-port™ connector, you cannot control the mobile terminal because you have already occupied the connection port (Pop-port™), so in this case you have to have jumper wires on production test points (Fbus Tx/Rx,GND).

Input Signals to FM Radio

After connecting a headset to the UHJ port to control the mobile terminal through Phoenix, you can see the following signals by turning on the FM radio in Phoenix.

- FMClk = Test Point (FM04) : 32 KHz/1.8 V
- FMWrEn = Test Point (FM03) : Write enable at 1.8 V
- FMCtrlClk = Test Point (FM02) : Control clock at 1.8 V
- FMCtrlDa = Test Point (FM01) : Control data at 1.8 V

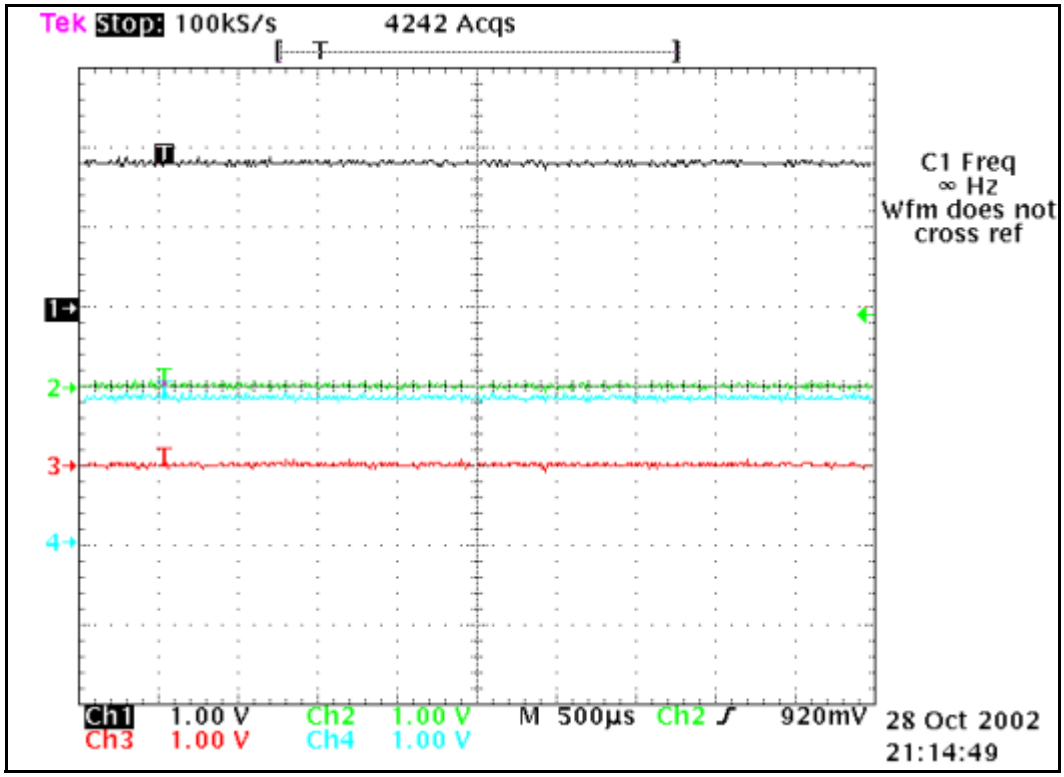


Figure 16: FM Radio signals before Radio on

- Ch1 : FMClk(32.768 KHz)
- Ch2 : FMWrEn
- Ch3 : FMctrlClk
- Ch4 : FMctrlDA

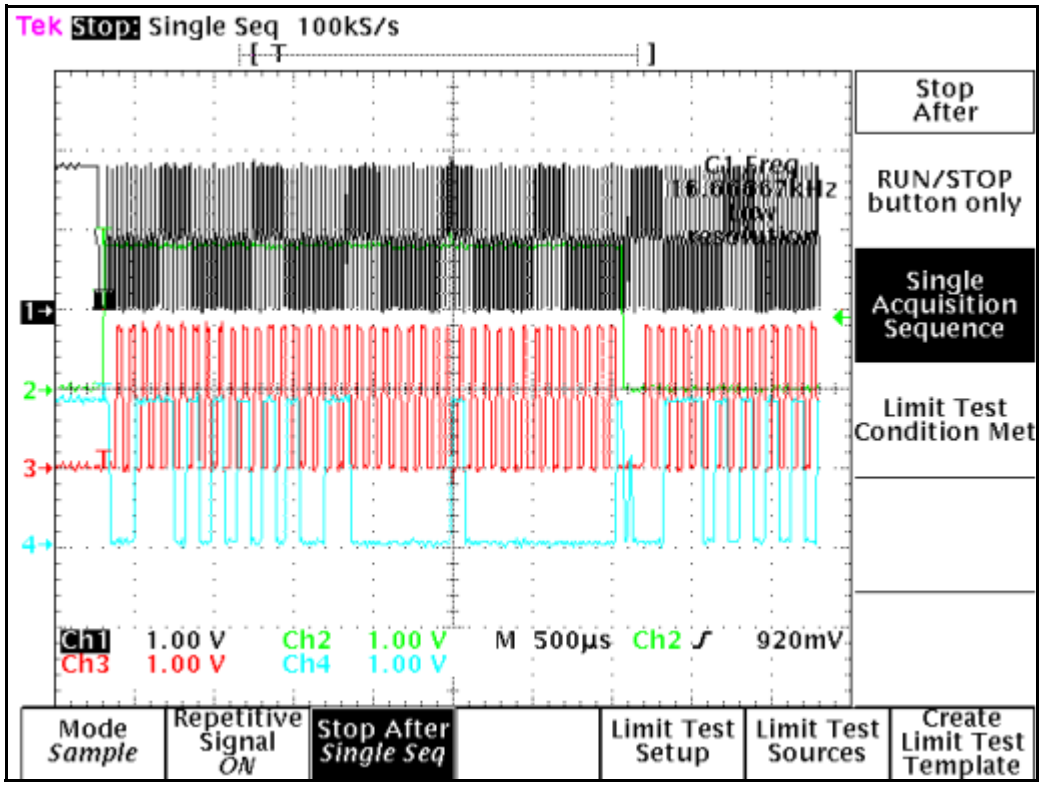


Figure 17: FM Radio signals after Radio on

FM Radio Testing with Pop-port™ Headset

1. Connect the Pop-port™ headset (HDS-3) to the bottom connector.
2. Select the "Radio" from the mobile terminal's User Interface Menu control.
3. Set a local radio station by selecting "Automatic Tuning" from the Radio Menu and pressing the UP arrow.
4. Listen for sound out of the headset.

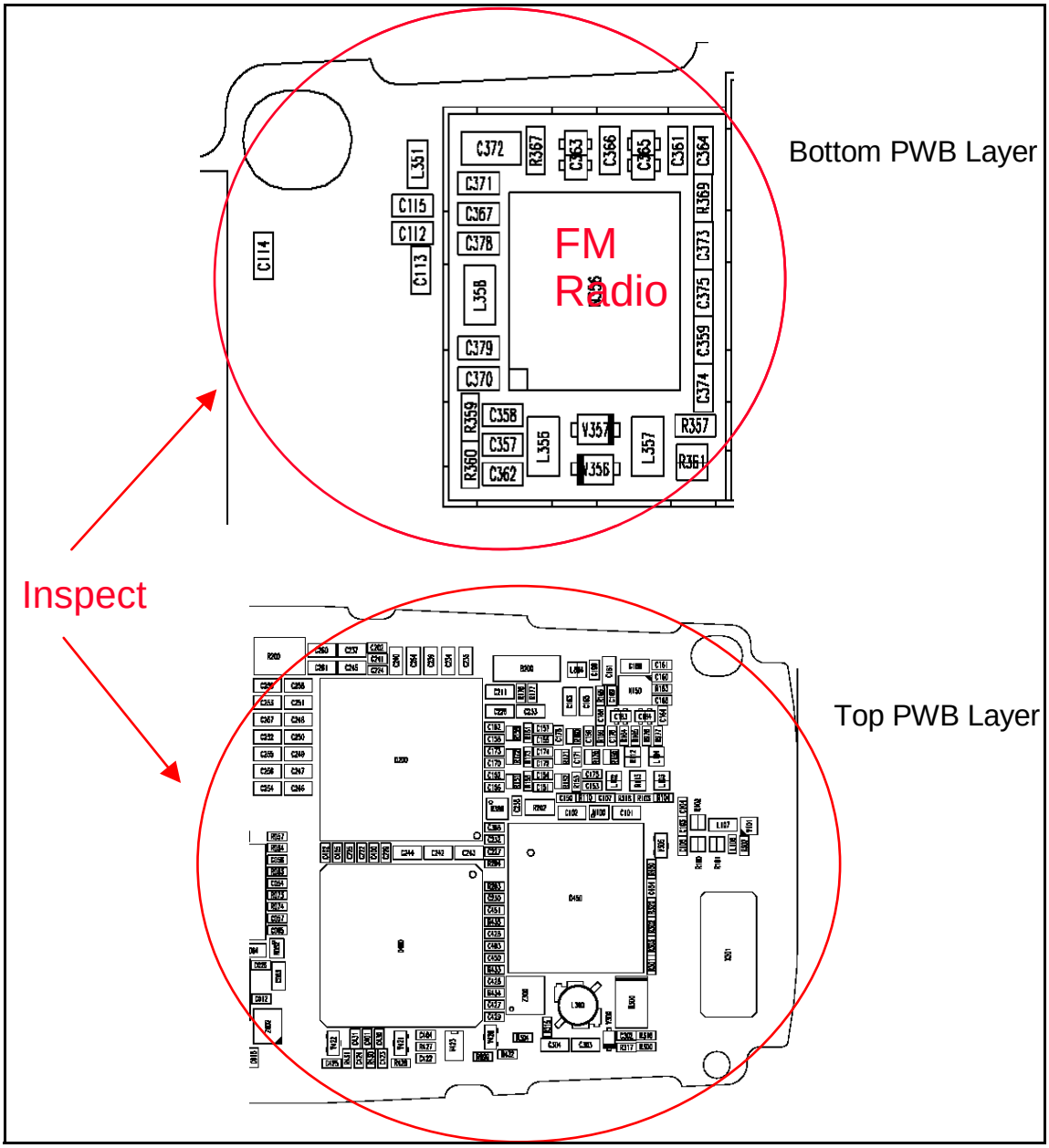
   If there is a signal present, continue with Step 5.

5. If there is no static or sound present, inspect all the FM radio circuits on the bottom PWB layer and refer to the *Baseband Description and Troubleshooting* chapter for audio amplifier troubleshooting.

FM Radio Testing with UHJ Headset

1. Disconnect the Pop-port™ headset (HDS-3) from the bottom connector and connect the UHJ headset.
2. Select the "Radio" menu from the mobile terminal's User Interface Menu control.
3. Set a local station by selecting "Automatic Tuning" from the Radio menu and then pressing the Up arrow.

4. Listen for sound out of the headset.



- If there is a signal present, the radio is functioning properly.
- If there is no static or sound present, then inspect the FM radio, Baseband circuits, and audio circuits.

Accessories

The 6585 supports Pop-port™ and Universal Headset accessories, differential and single-ended, respectively. Detection of the Pop-port™ accessories is done through the ACI signal where the Universal Headset is detected on GenIO (4).

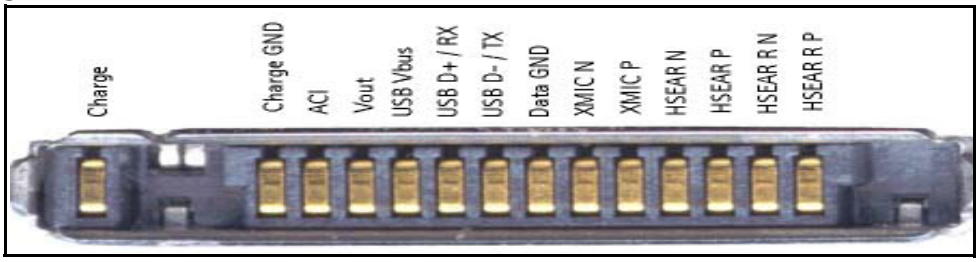


Figure 18: Pop-port™ connector pin out

Figure 19: The pin out on the Pop-port™ connector is as follows:

- Charger
- Charger GND
- ACI
- Vout
- USB Vbus
- USB D+ / Fbus Rx
- USB D- / Fbus Tx
- Data GND
- XMic N
- XMic P
- HSear N
- HSear P
- HSear R N
- HSear R P

You can perform the following in Pop-port™ accessories:

- Charging
- Accessory detection
- FBUS communication
- USB communication
- Fully differential audio interface for mono- and stereo outputs

Charging

Charging through Pop-port™ is accomplished in the same manner as through the charger connector. Pin 1 of the Pop-port™ is physically connected to the charger connector. When the mobile terminal is connected to a desktop charger (e.g., DCV-15), it charges in the same manner as it does with the charger connector.

Figure 20 shows the actual charging sequence. The channels on the diagram are:

- CH1 = Charging current across the .22 Ohm (R200) resistor on UEMEK
- CH2 = Charger voltage measure at V100
- CH3 = Battery voltage measure at R200
- CH4 = PURX

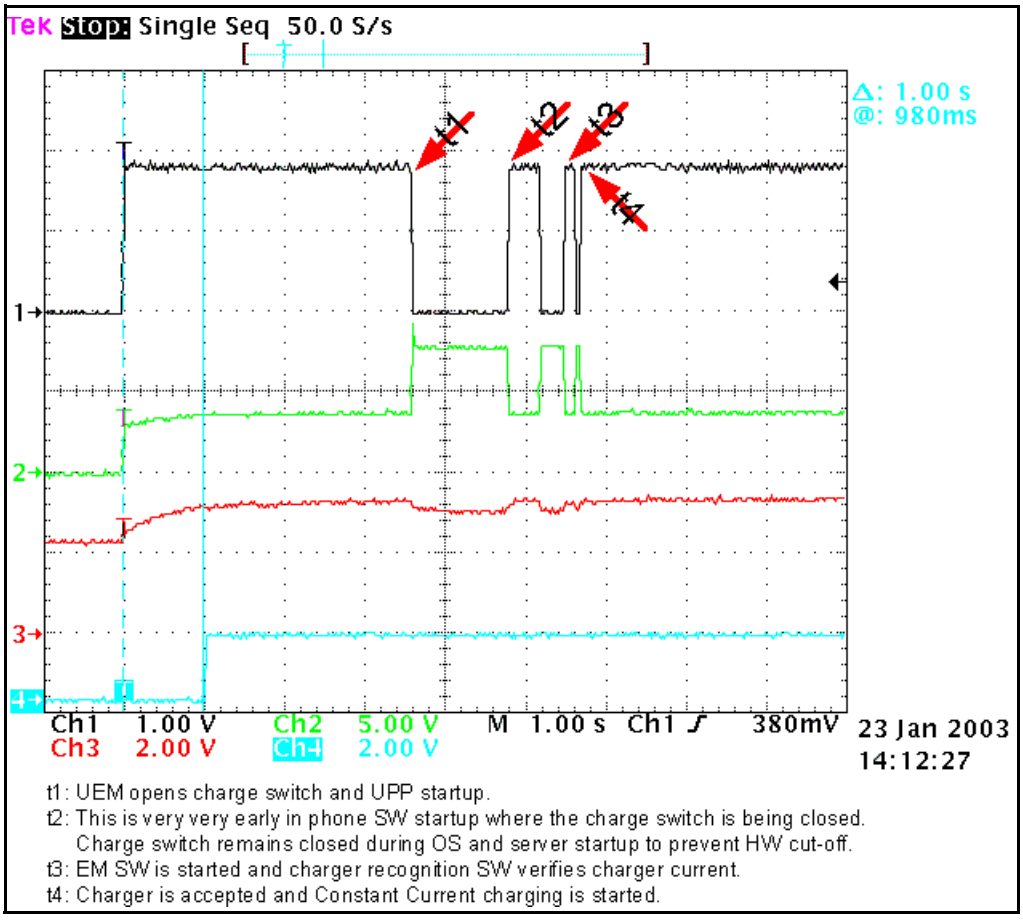


Figure 20: Charging sequence

In Channel 4, PURX is released, which this indicates when the mobile terminal operation goes from reset mode to power-on mode.

Pop-port™ Headset Detection

Accessory detection on Pop-port™ is done digitally. The pins used for accessory detection are:

- Pin 2 (Charge GND)
- Pin 3 (ACI)
- Pin 4 (Vout))

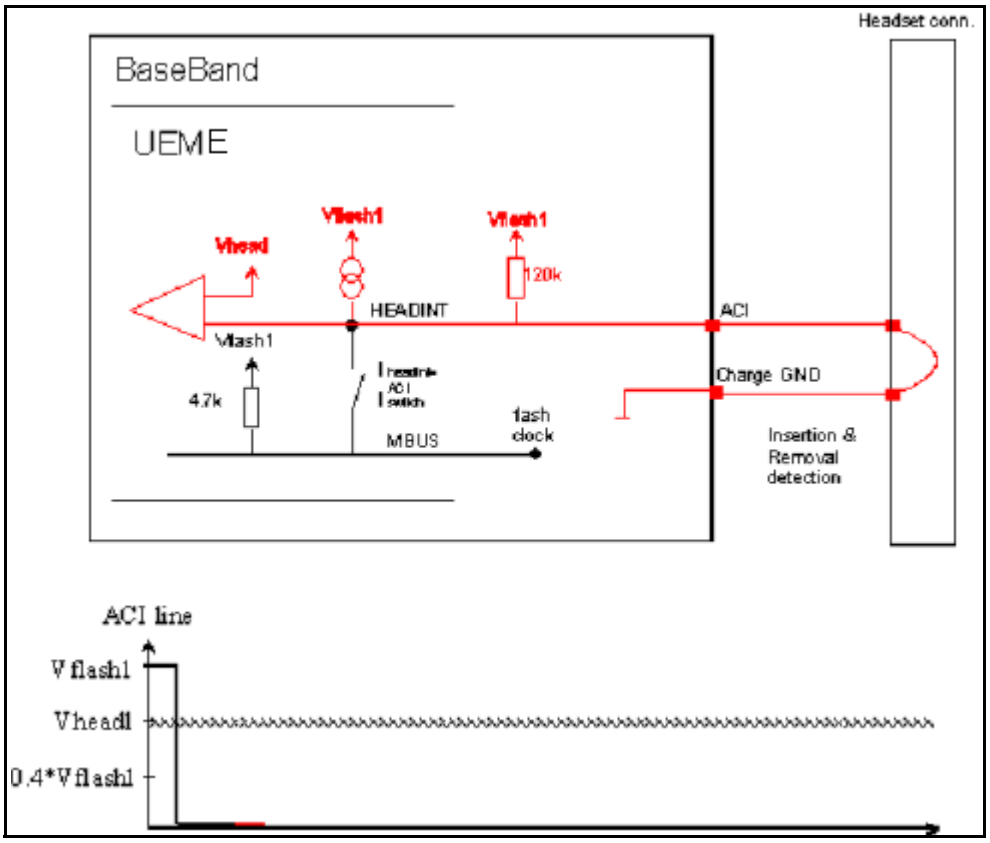


Figure 21: Waveform showing Pop-port™ accessory detection

FBus Detection

FBus communication in Pop-port™ is done through the following lines:

- Pin 2 (Charge GND)
- Pin 3 (ACI)
- Pin 4 (Vout)
- Pin 6 (FBus Rx)
- Pin 7 (FBus Tx)

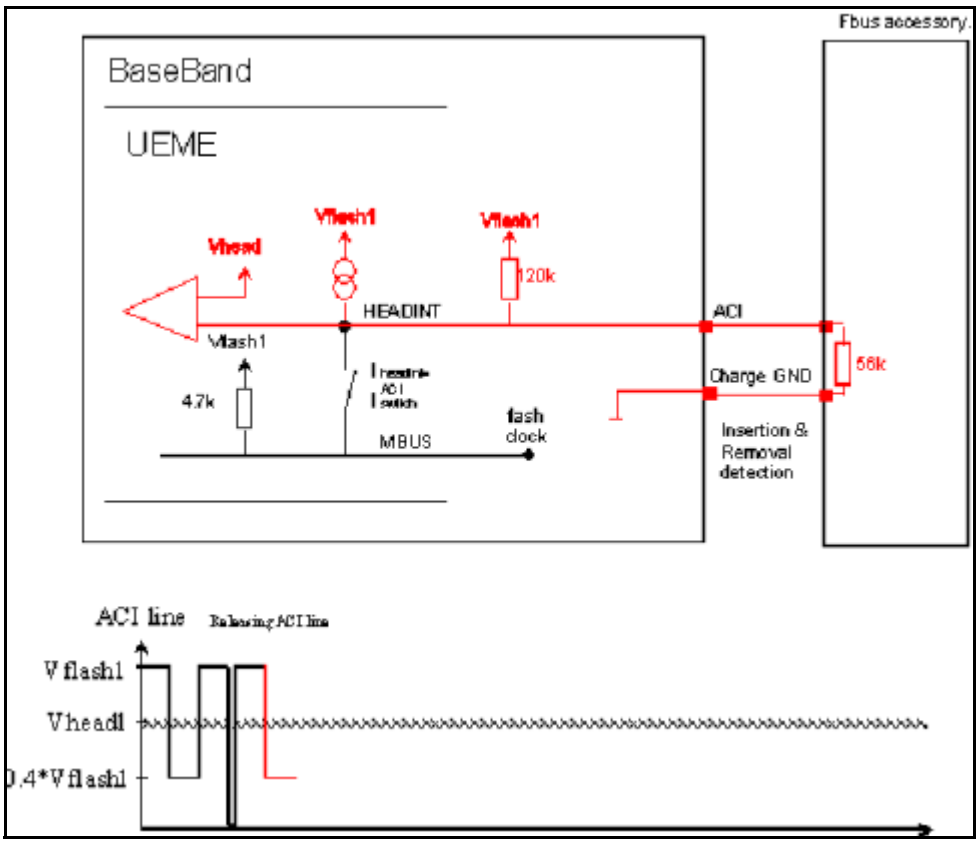


Figure 22: Waveform showing Pop-portT™ FBus communication

Accessory Detection Though ACI

USB and audio (mono or stereo) and FM radio communication in Pop-port™ is done through the following signals:

Table 5: Accessory Detection Signals

USB	Audio/FM
Pin 5 (USB Vbus)	Pin 9 (XMic N)
Pin 6 (USB +)	Pin 10 (SMIC P)
Pin 7 (USB -)	Pin 11 (HSEAR N)
Pin 8 (Data GND)	Pin 12 (HSEAR P)
	Pin 13 (HSEAR R N)
	Pin 14 (HSEAR R P)

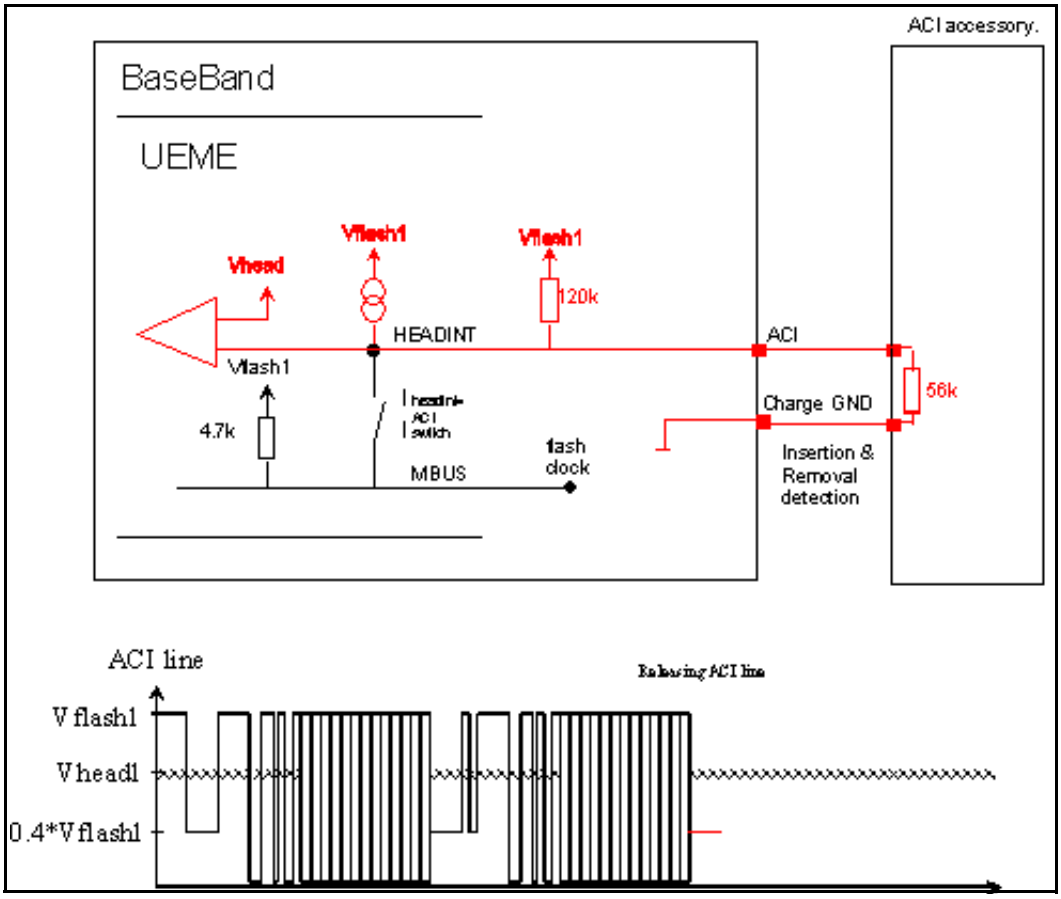


Figure 23: Waveform showing accessory detection through ACI

RUIM (SIM CARD)

The mobile terminal supports SIM CARD. Use the waveform in Figure 24 to verify that the sim_vcc, sim_i/o, cim_clk, and sim_rst signals are activated in the correct sequence at power up. This picture may be taken when the SIM CARD is installed on the mobile terminal to measure the signals when the mobile terminal is turned on. The figure shows the proper waveforms when the interface is working.

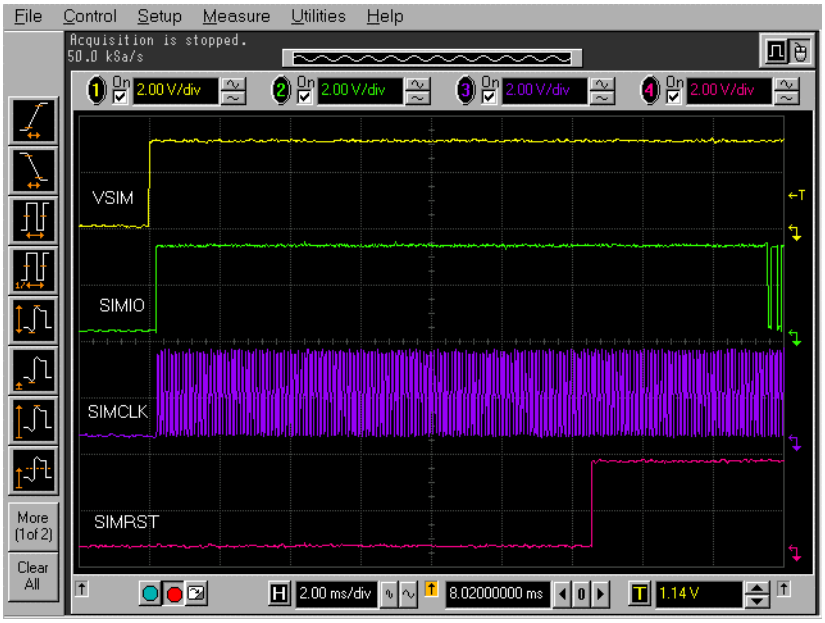
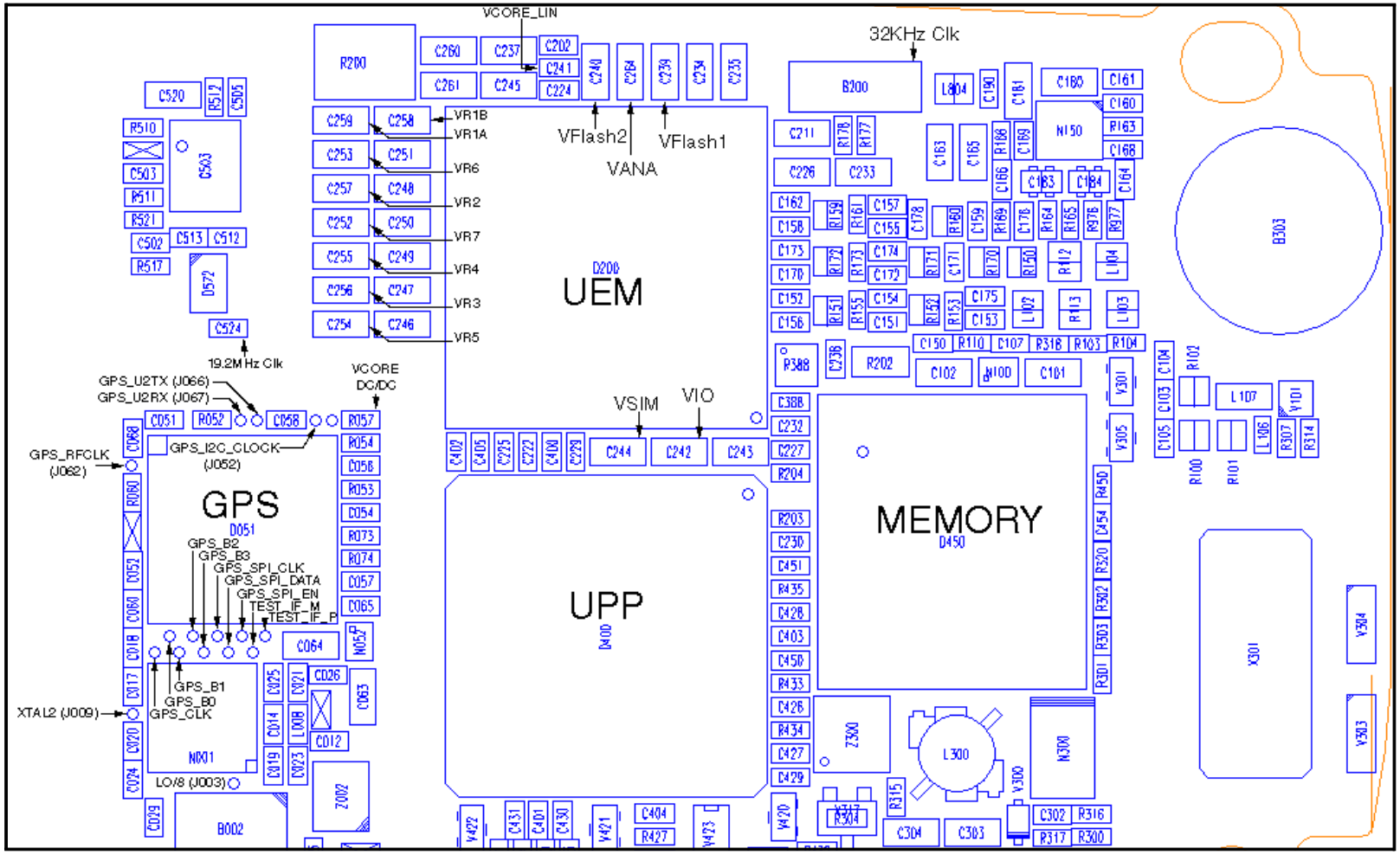
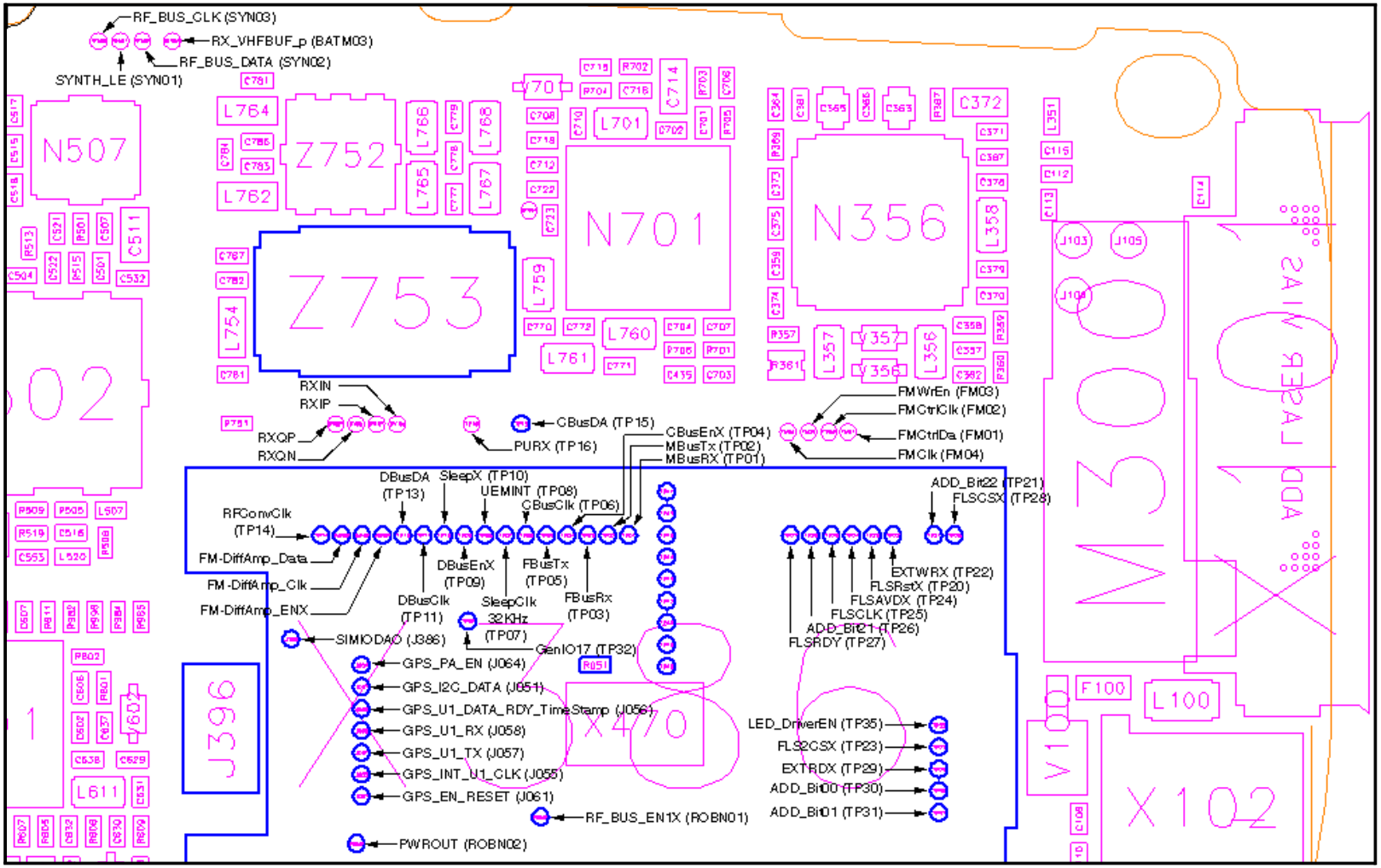


Figure 24: RUIM signal waveform

Test Points





Troubleshooting

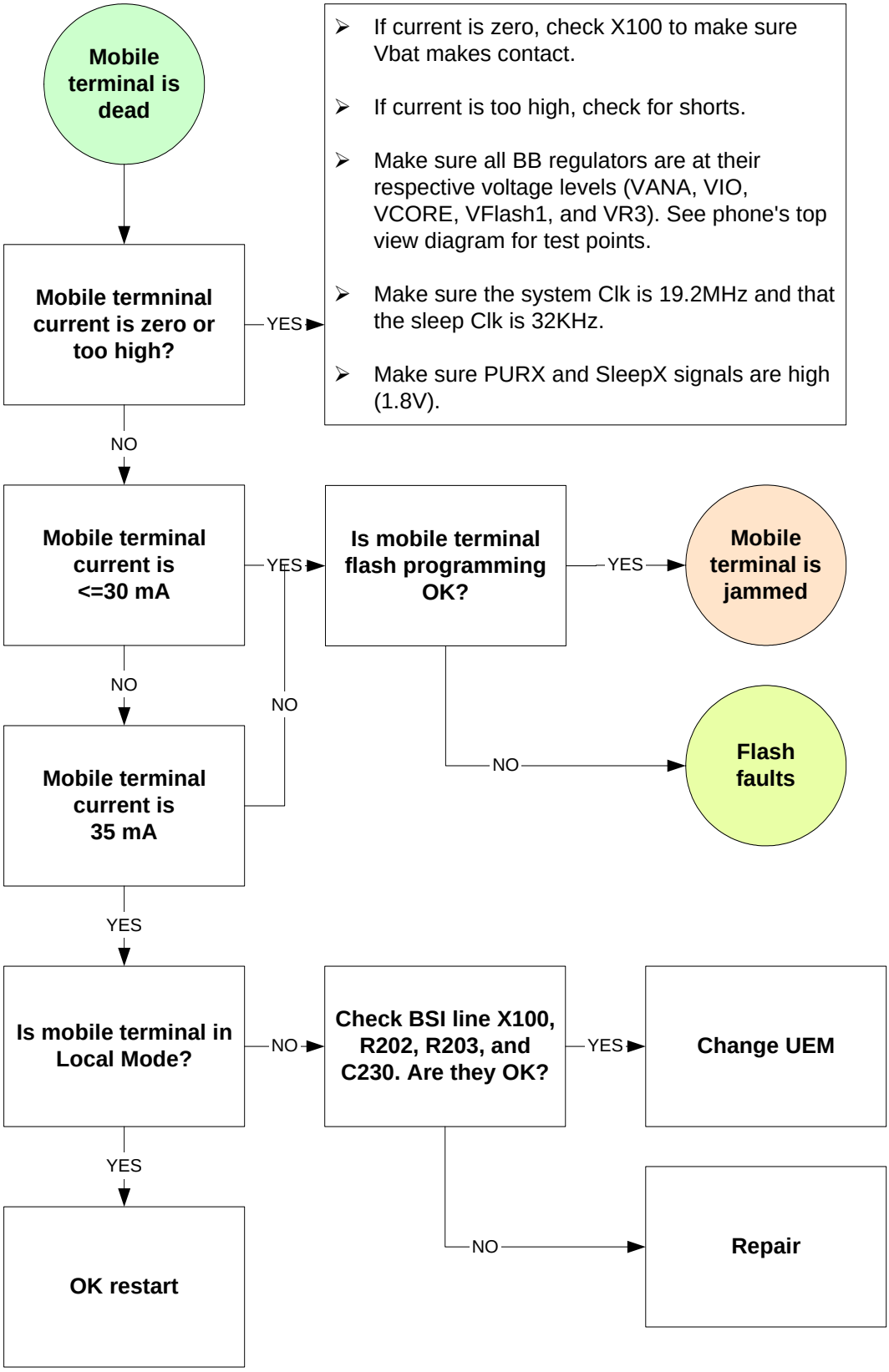
The following hints allow you to find the cause of the problem when the circuitry seems to be faulty. Troubleshooting instructions are divided into the following sections:

- "Mobile Terminal is Dead"
- "Flash Programming Does Not Work"
- "Power Does Not Stay on or the Mobile Terminal is Jammed"
- "Charger Faults"
- "Audio Faults"
- "Display Faults"
- "Keypad Faults"
- "FM Radio Faults"
- "GPS Module"

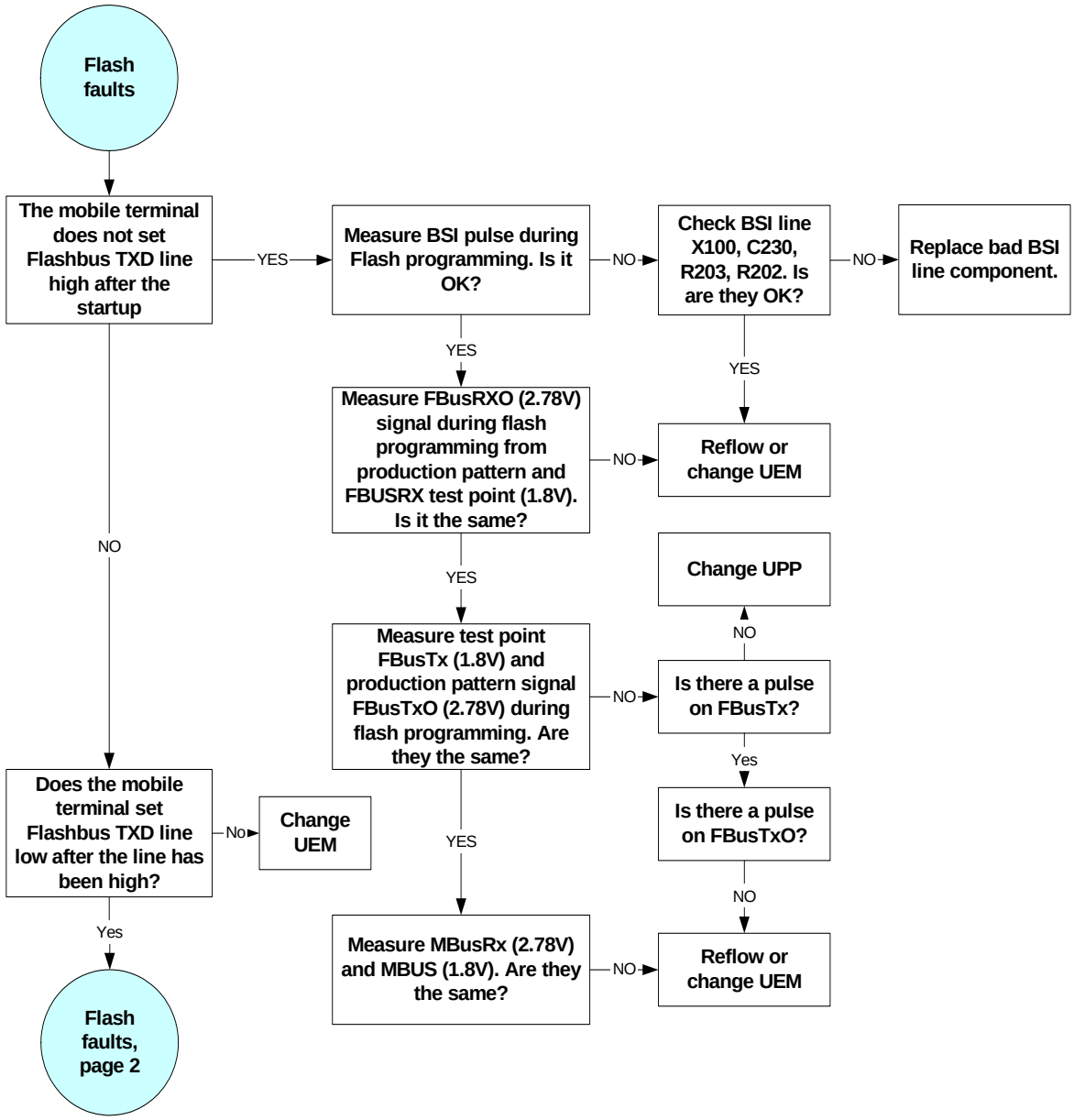
First, carry out a through visual check of the module. Ensure in particular that:

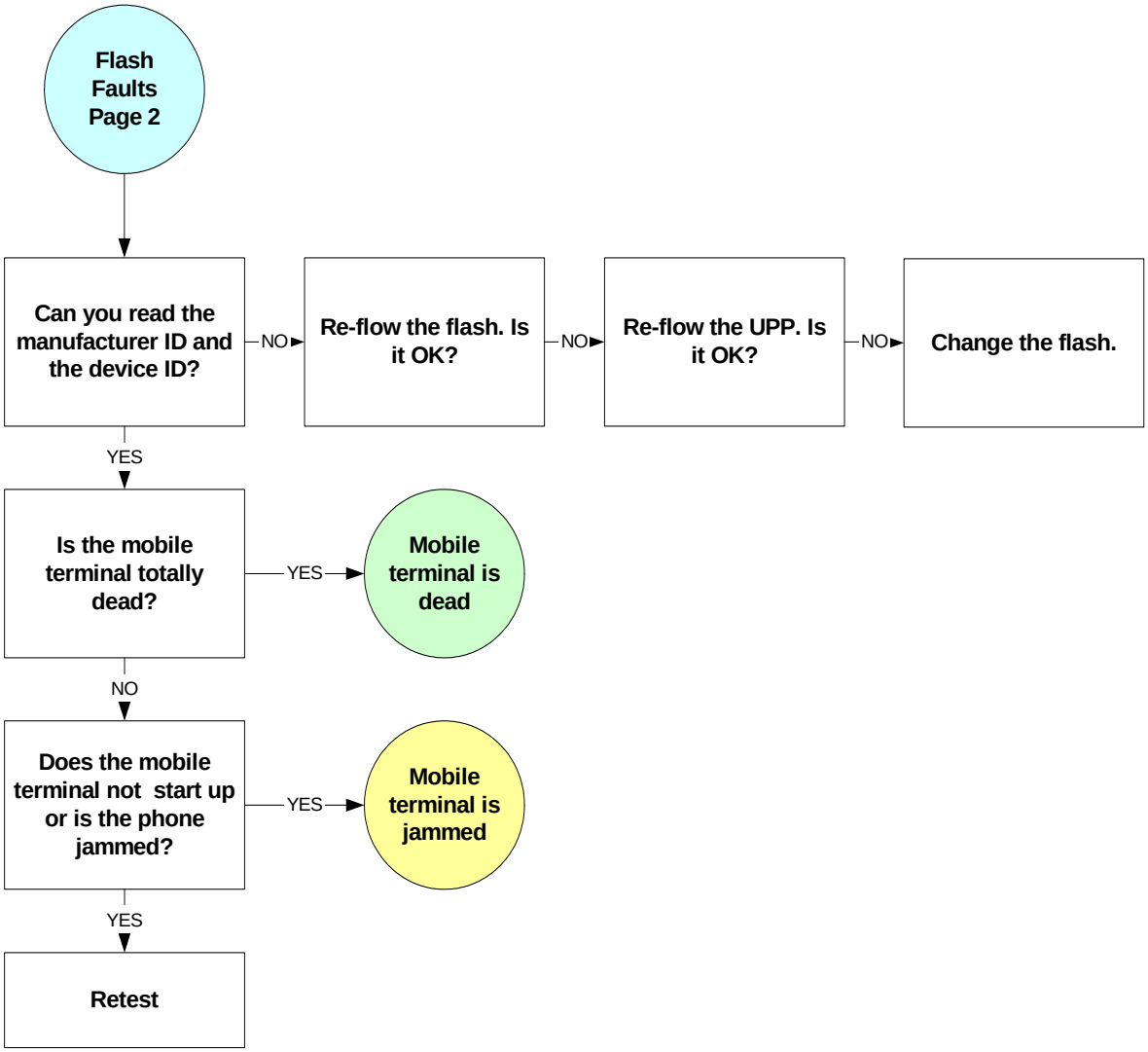
- There are no mechanical damages
- Soldered joints are OK
- ASIC orientations are OK

Mobile Terminal is Dead

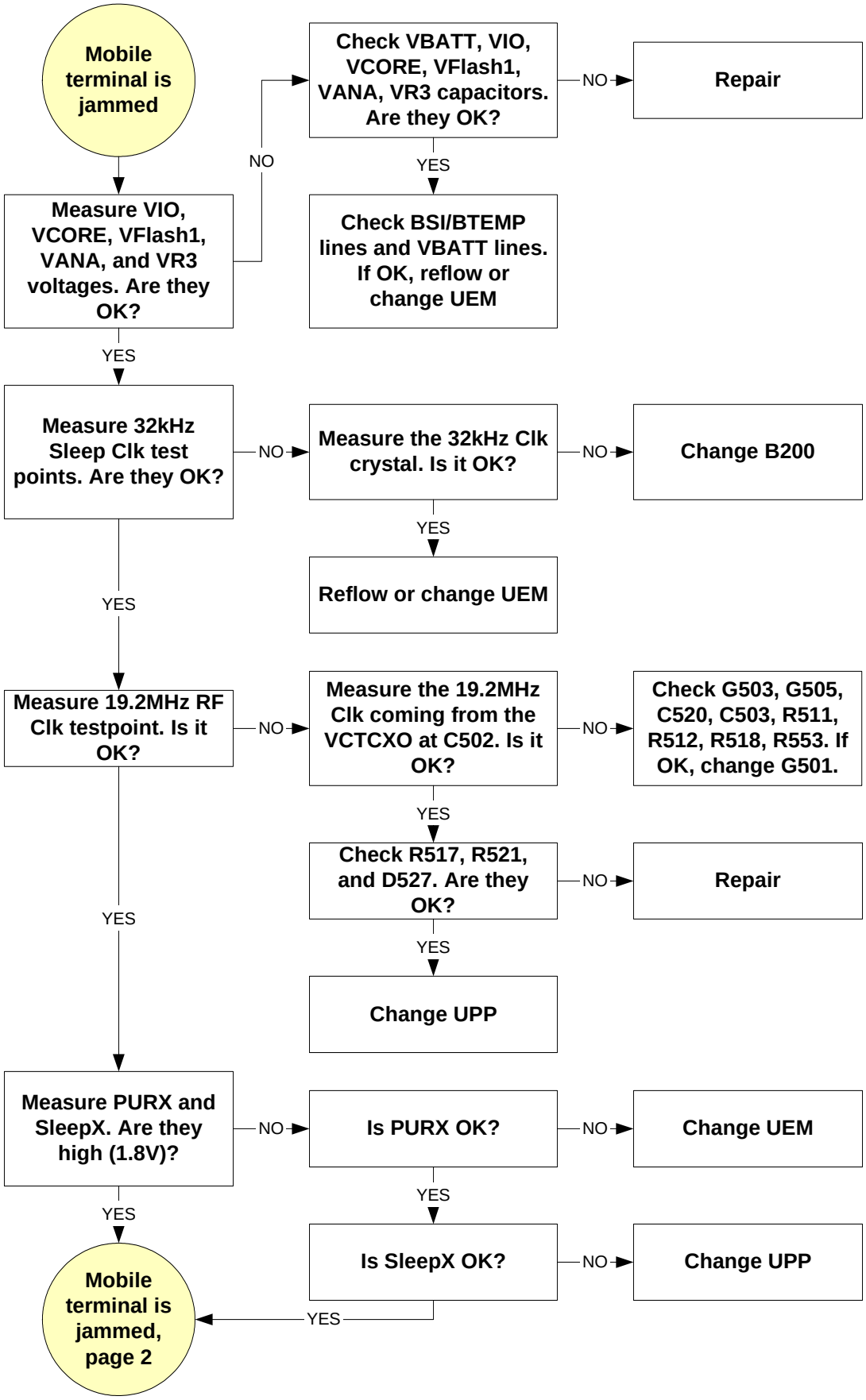


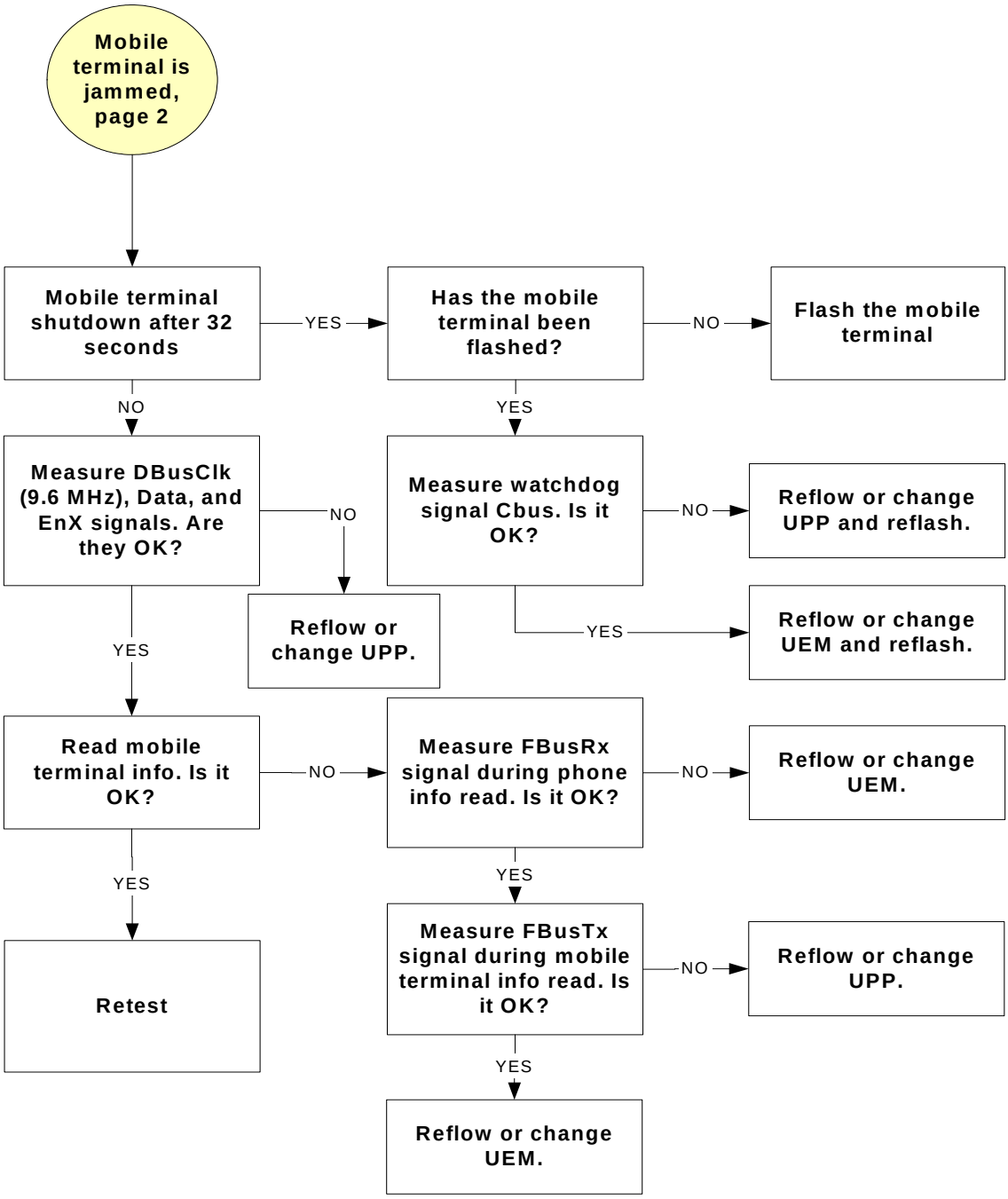
Flash Programming Does Not Work



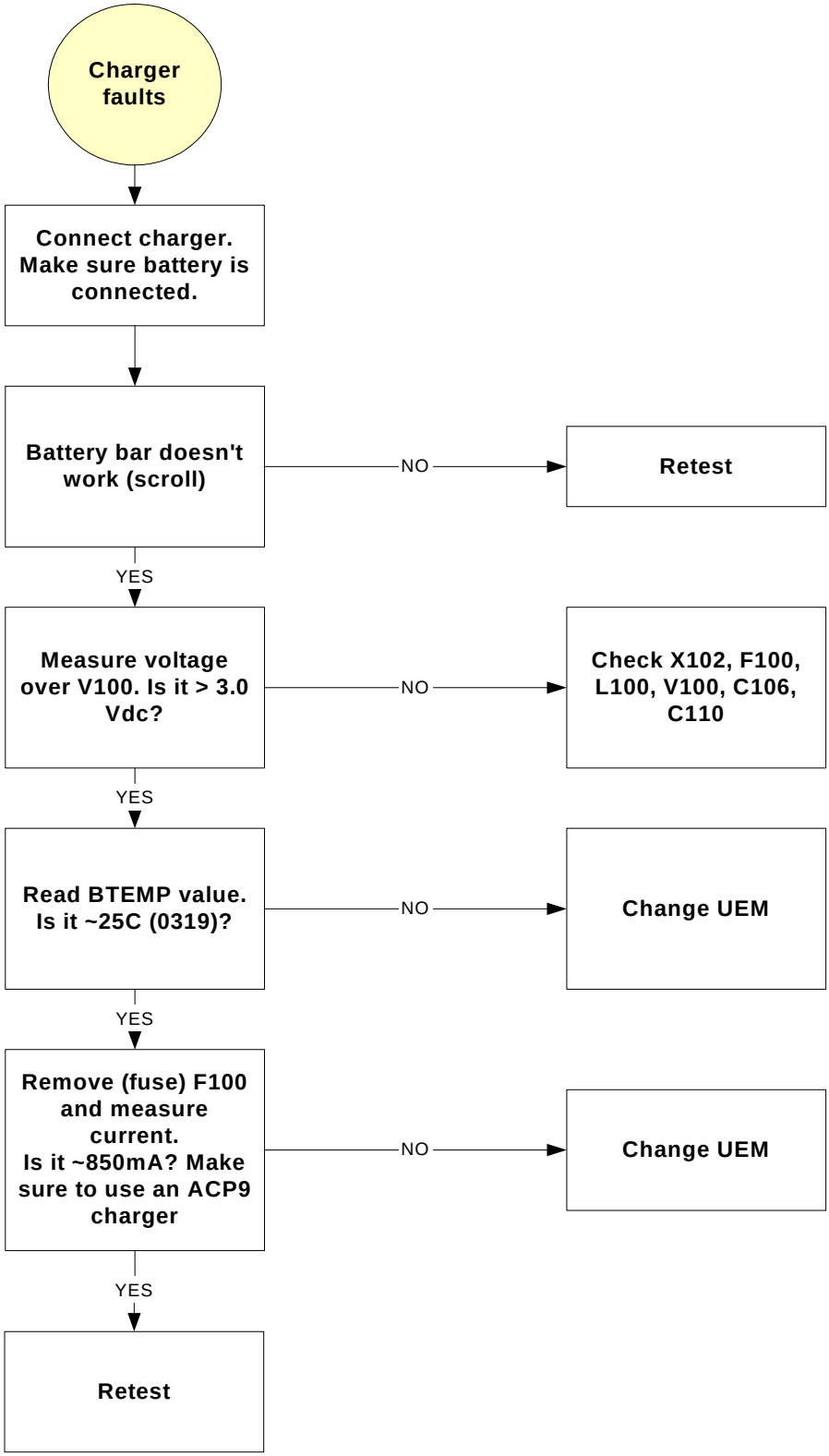


Power Does Not Stay on or the Mobile Terminal is Jammed



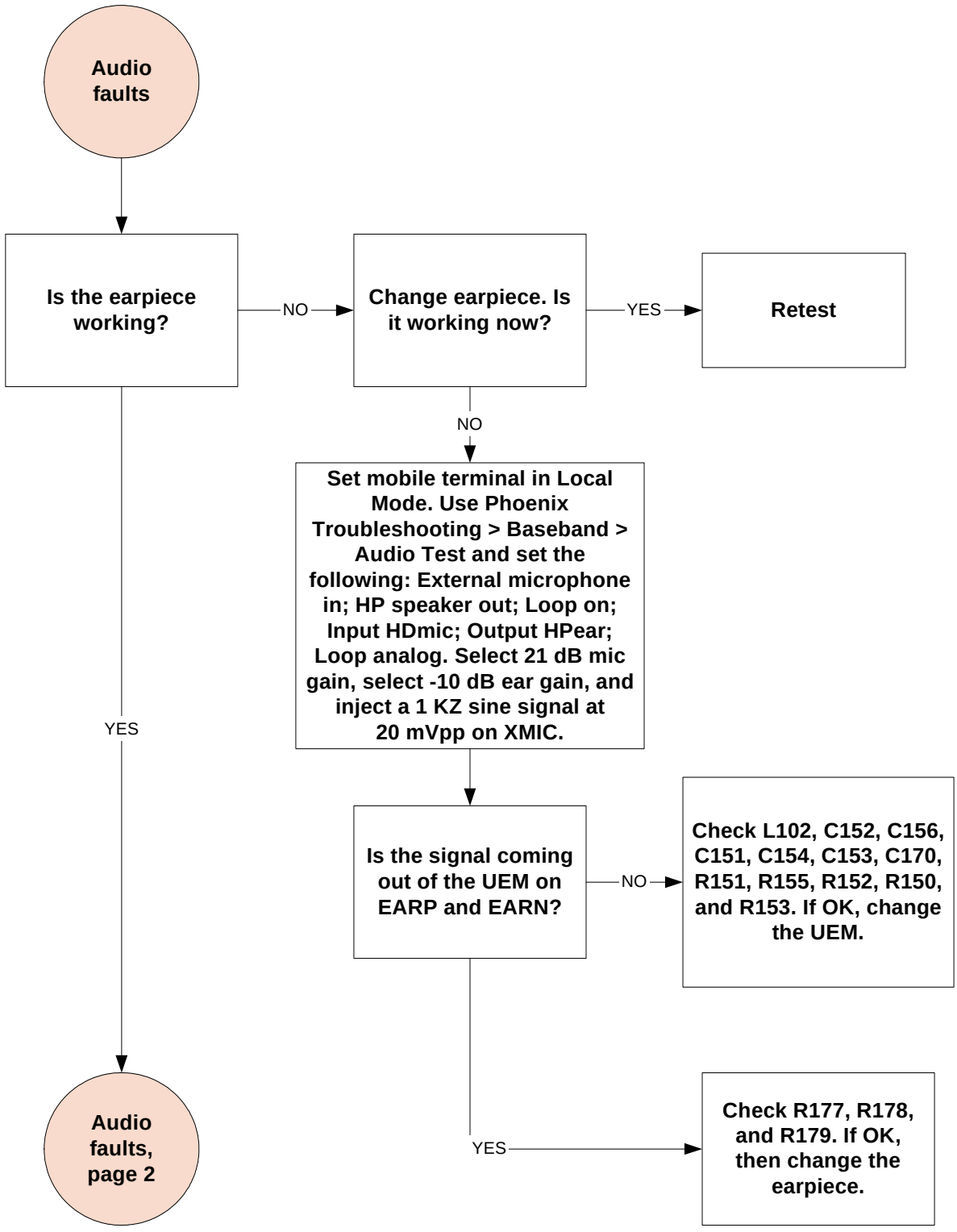

Mobile terminal is jammed, page 2
Mobile terminal shutdown after 32 seconds
YES
Has the mobile terminal been flashed?
NO
Flash the mobile terminal
NO
YES
Measure DBusClk (9.6 MHz), Data, and EnX signals. Are they OK?
NO
Measure watchdog signal Cbus. Is it OK?
NO
Reflow or change UPP and reflash.
Reflow or change UPP.
YES
Reflow or change UEM and reflash.
YES
Read mobile terminal info. Is it OK?
NO
Measure FBusRx signal during phone info read. Is it OK?
NO
Reflow or change UEM.
YES
YES
Measure FBusTx signal during mobile terminal info read. Is it OK?
NO
Reflow or change UPP.
Retest
YES
Reflow or change UEM.

Charger Faults

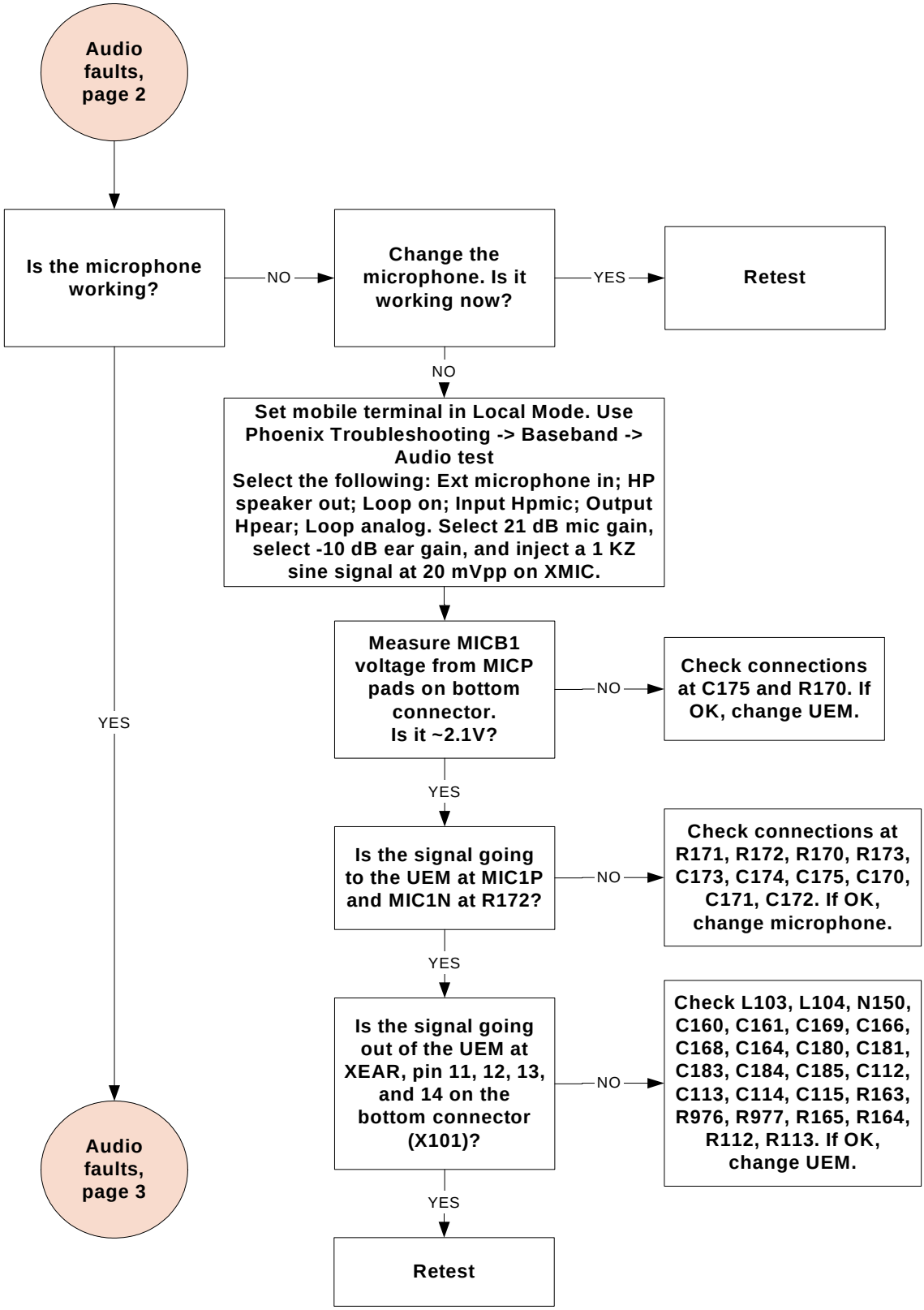


Audio Faults

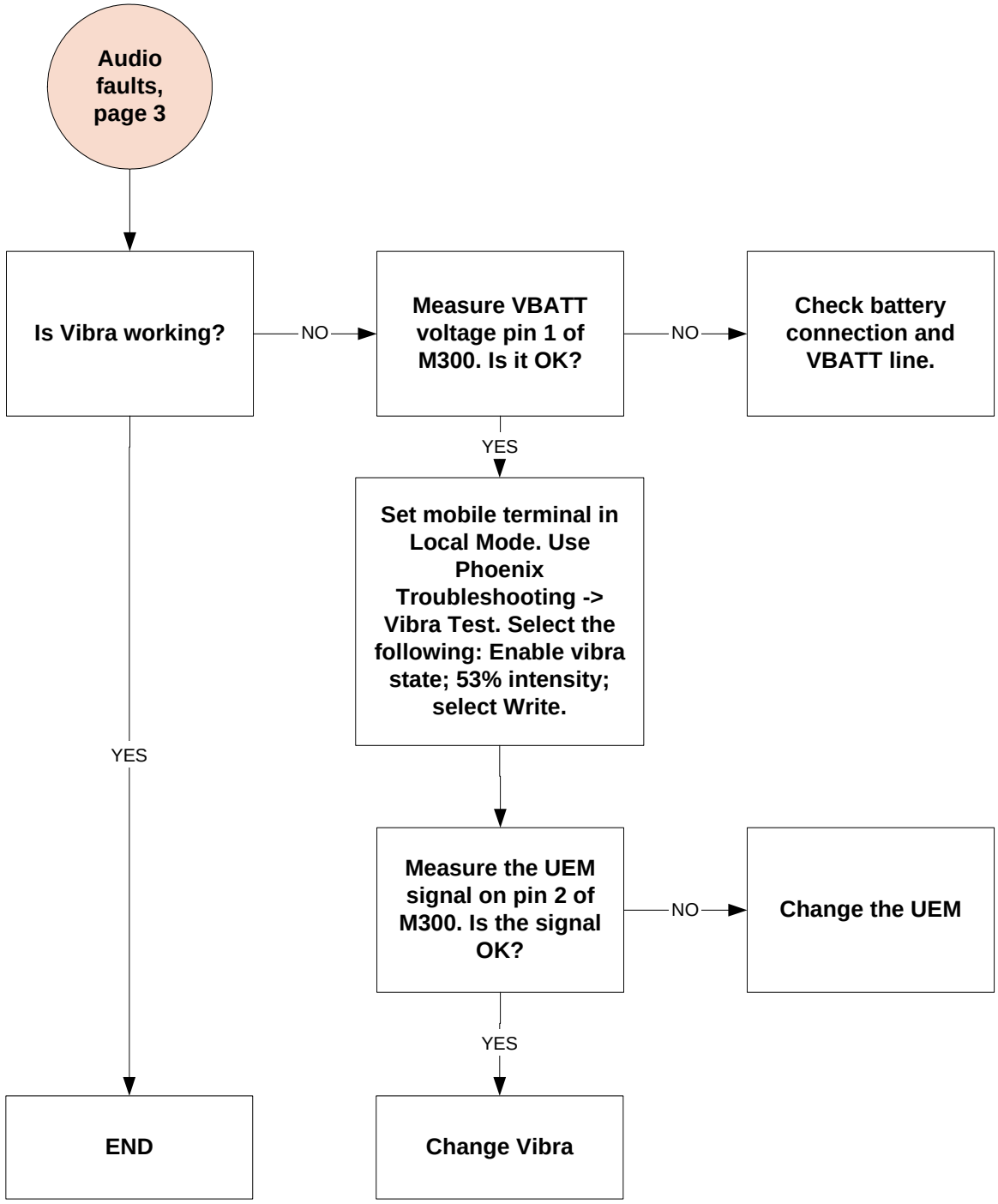
Earpiece



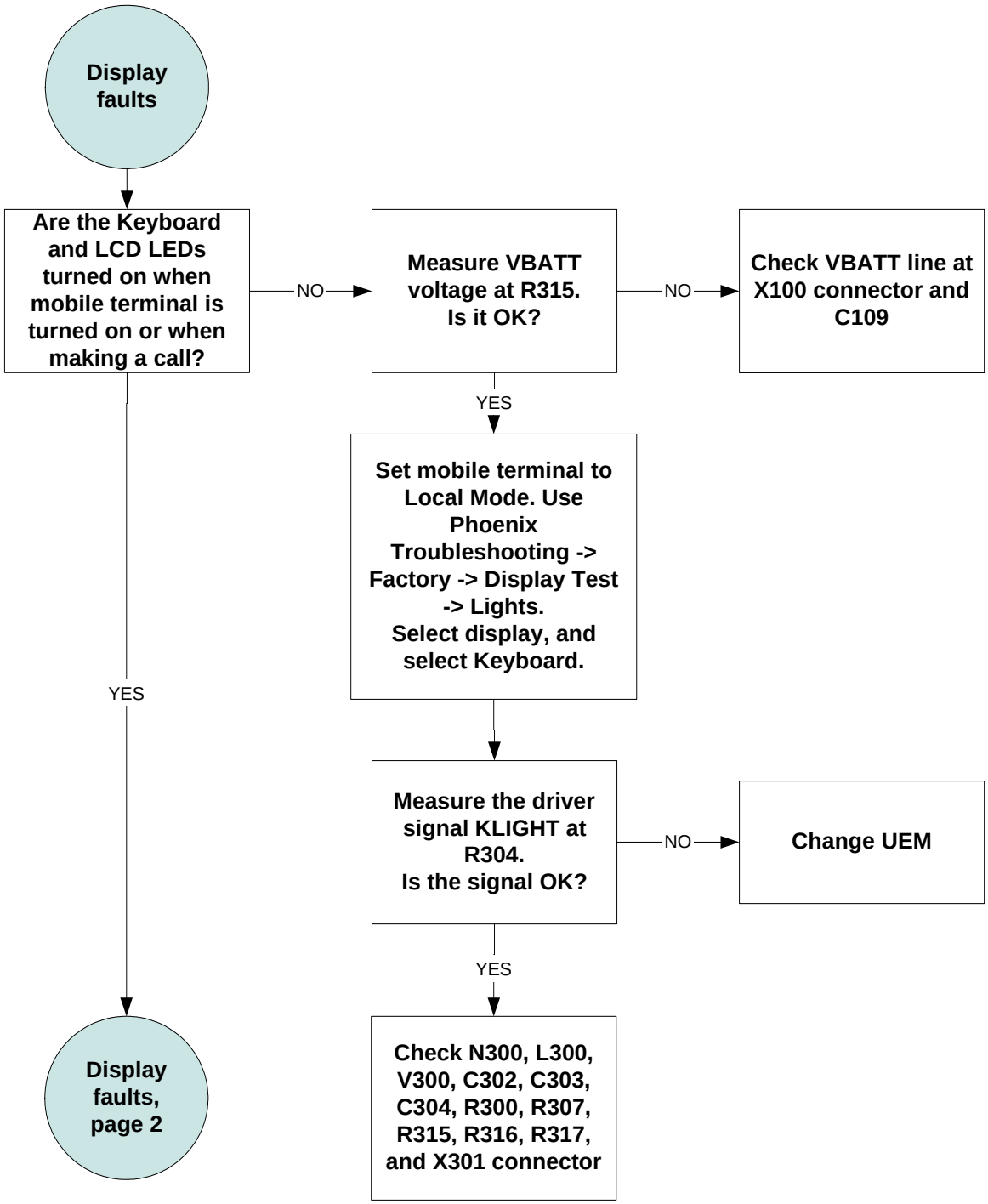
Microphone

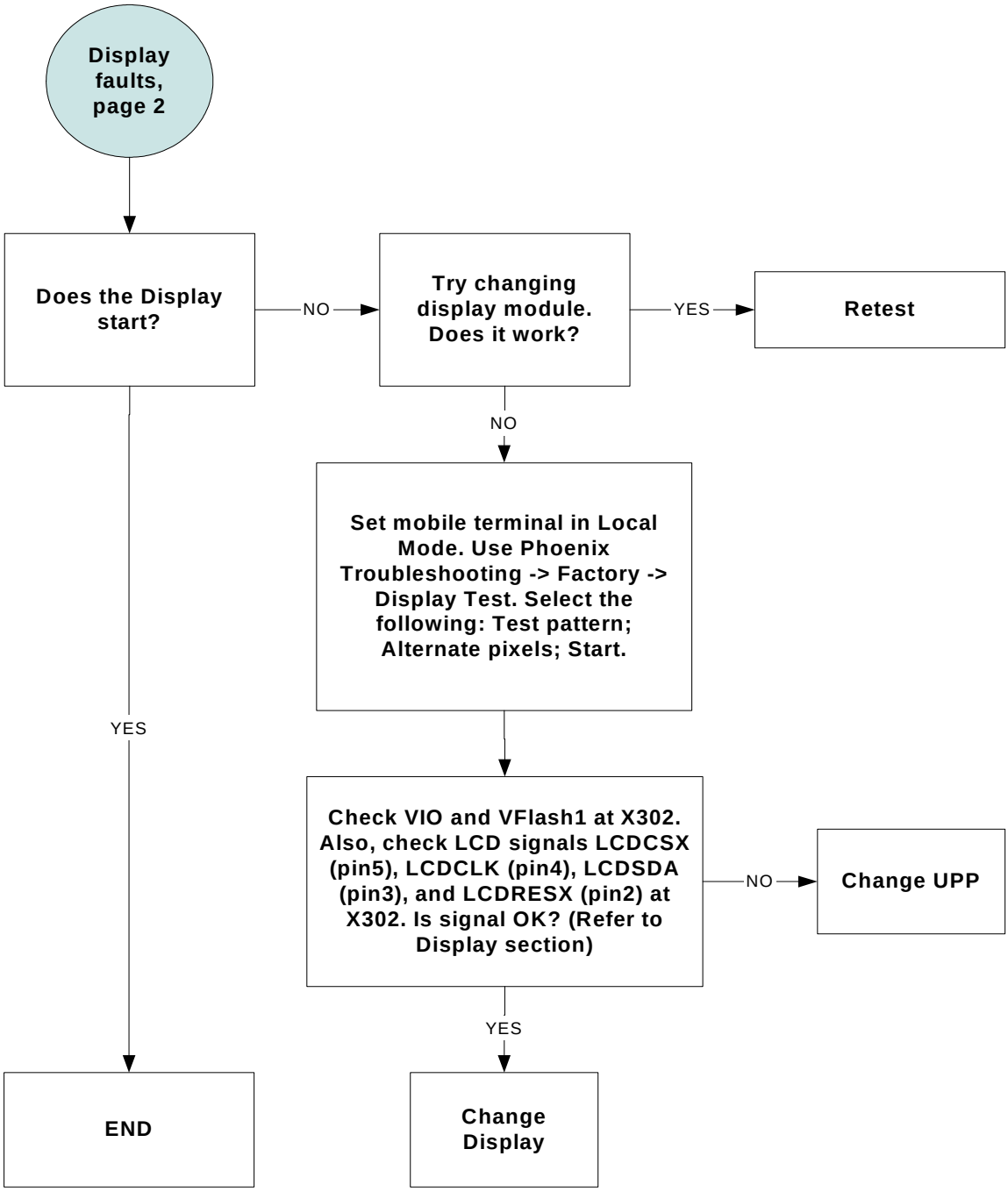


Vibra



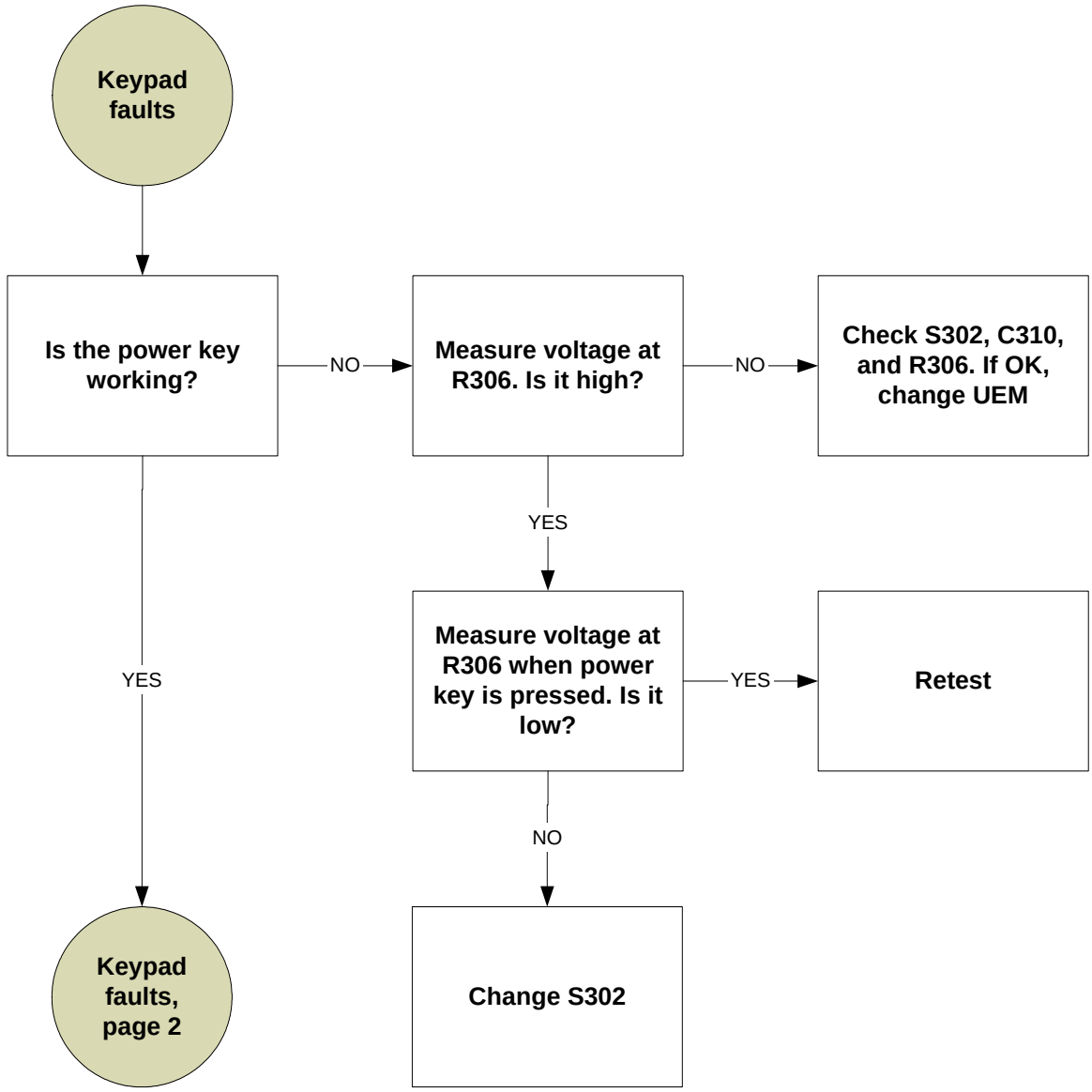
Display Faults



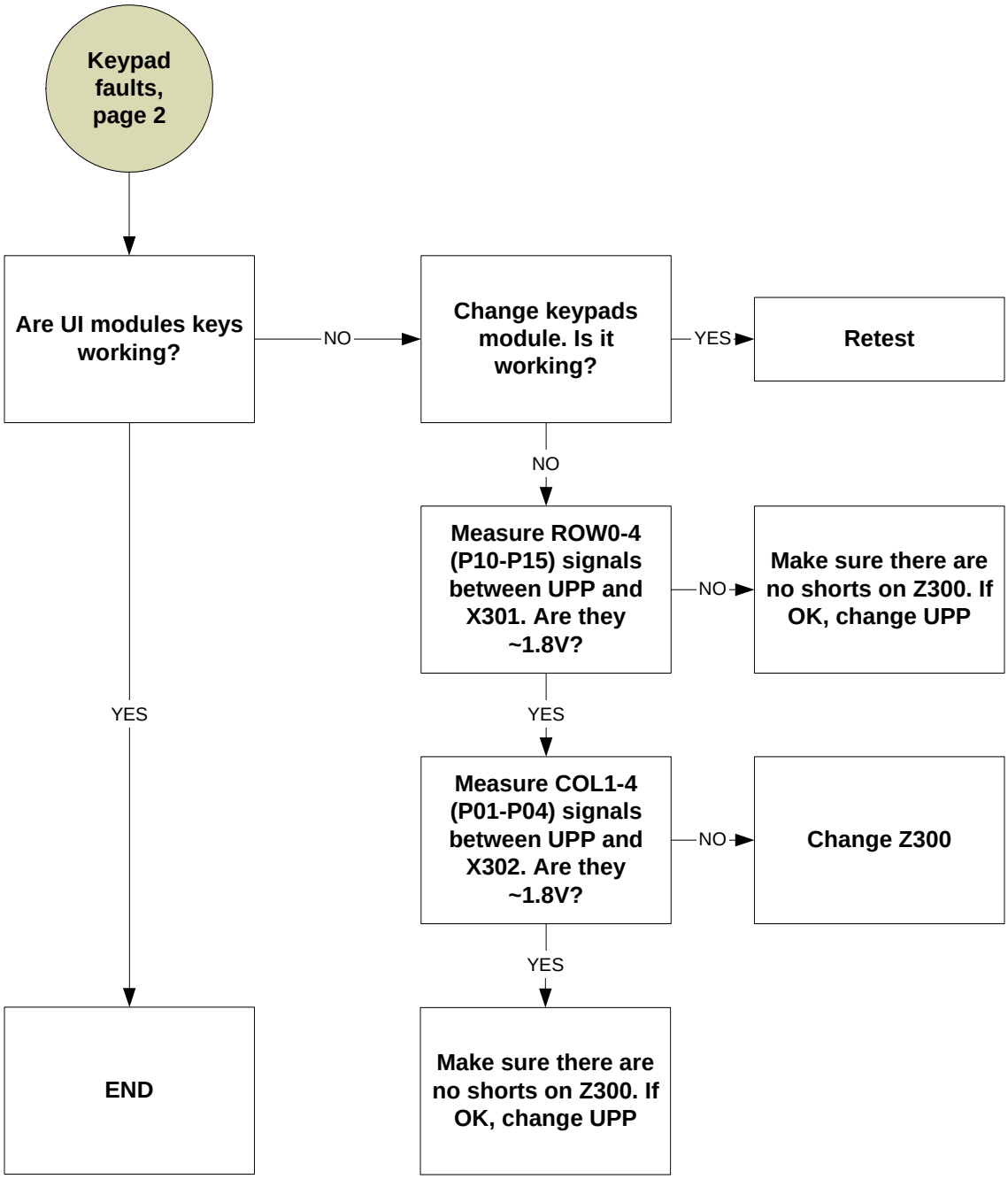

Display faults, page 2
Does the Display start?
NO
Try changing display module. Does it work?
YES
Retest
NO
Set mobile terminal in Local Mode. Use Phoenix Troubleshooting -> Factory -> Display Test. Select the following: Test pattern; Alternate pixels; Start.
YES
Check VIO and VFlash1 at X302. Also, check LCD signals LCDCSX (pin5), LCDCLK (pin4), LCDSDA (pin3), and LCDRESX (pin2) at X302. Is signal OK? (Refer to Display section)
NO
Change UPP
YES
END
Change Display

Keypad Faults

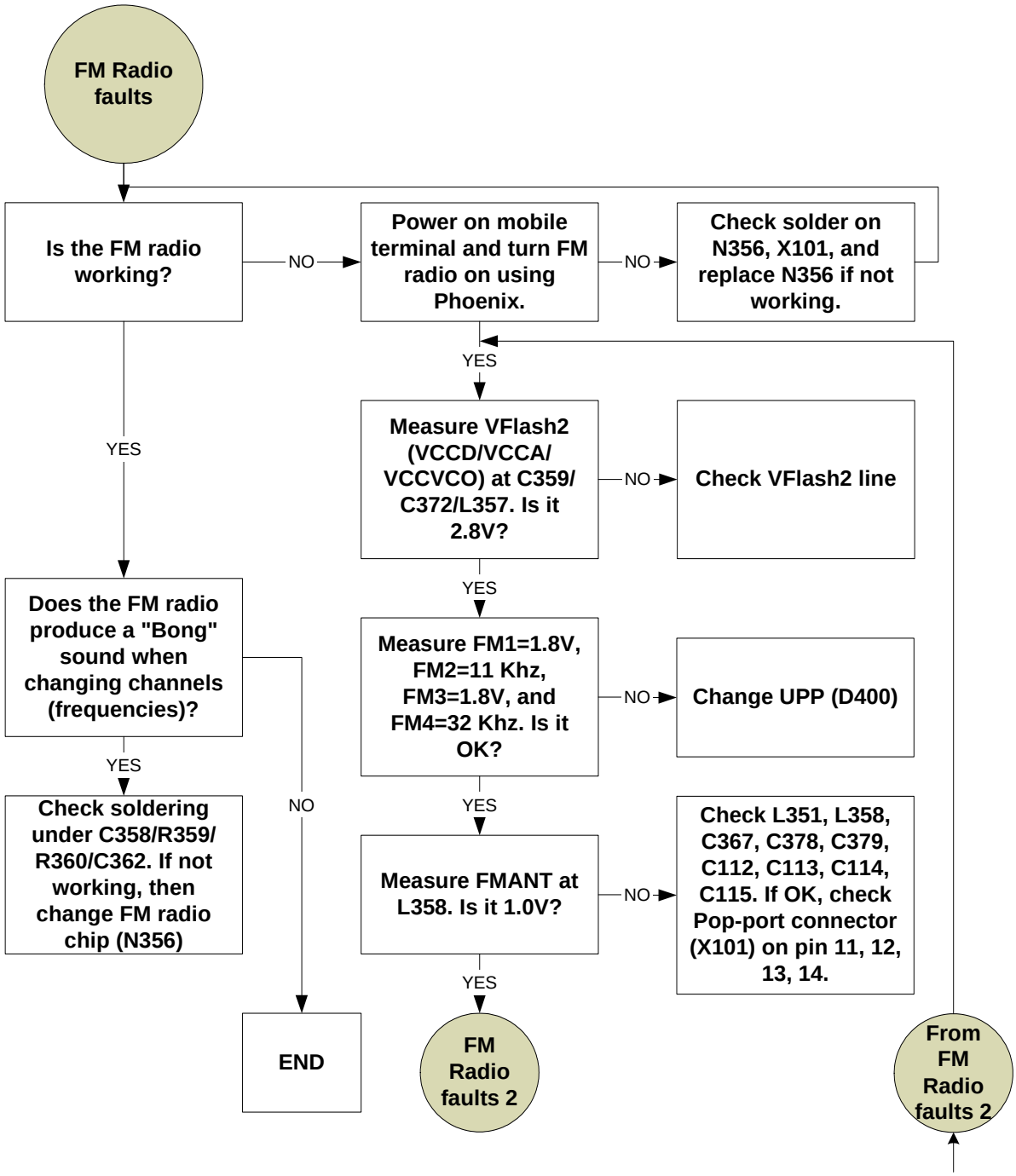
Power Key

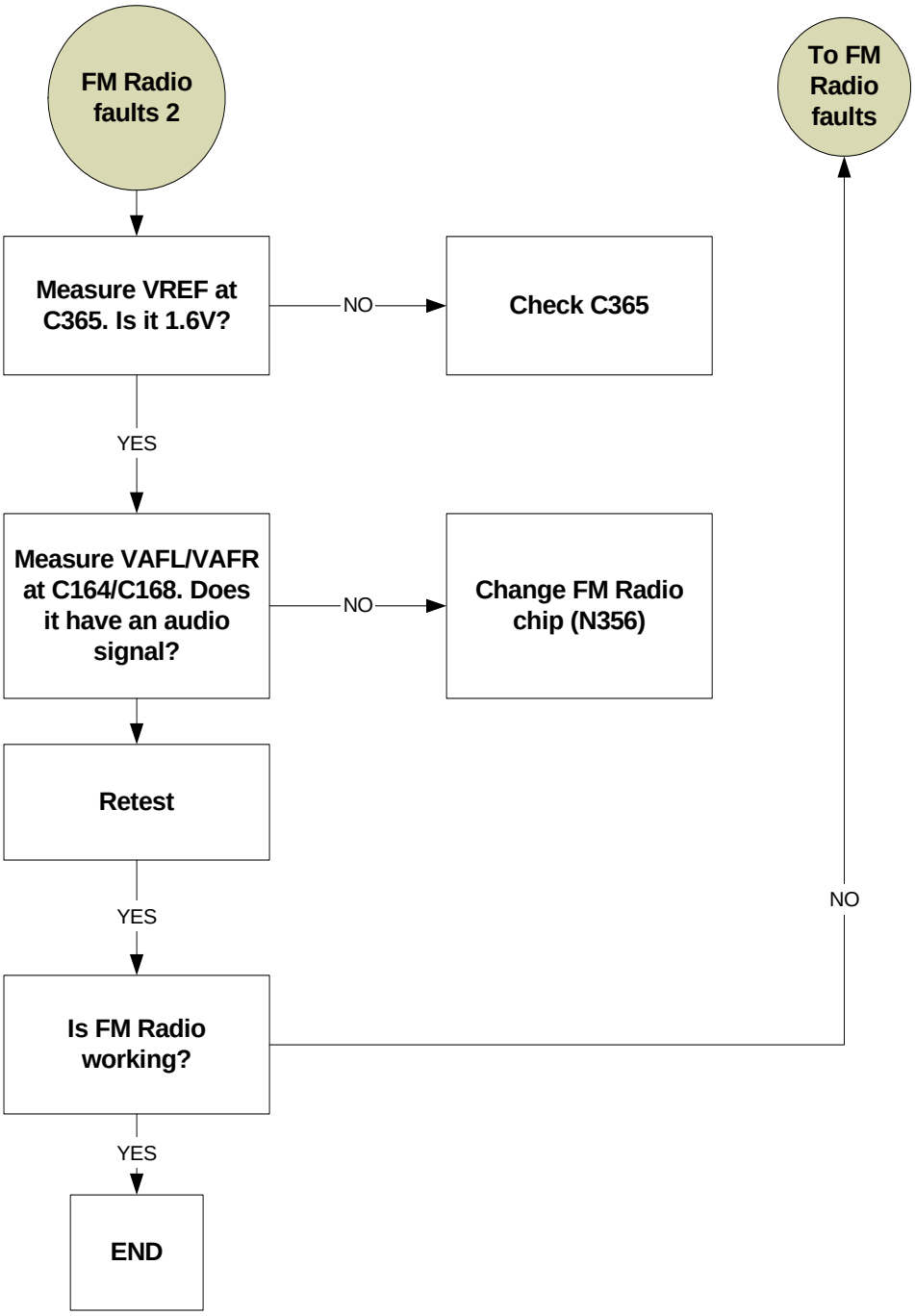


UI Modules



FM Radio Faults




FM Radio faults 2
To FM Radio faults
Measure VREF at C365. Is it 1.6V?
NO
Check C365
YES
Measure VAFL/VAFR at C164/C168. Does it have an audio signal?
NO
Change FM Radio chip (N356)
Retest
YES
NO
Is FM Radio working?
YES
END

GPS Module

The GPS circuitry utilizes RF signals from satellites stationed in geosynchronous orbit to determine longitude and latitude of the handset. The GPS circuitry is completely separate of the CE circuitry and is located almost exclusively on the secondary side of the PWB underneath the display module.

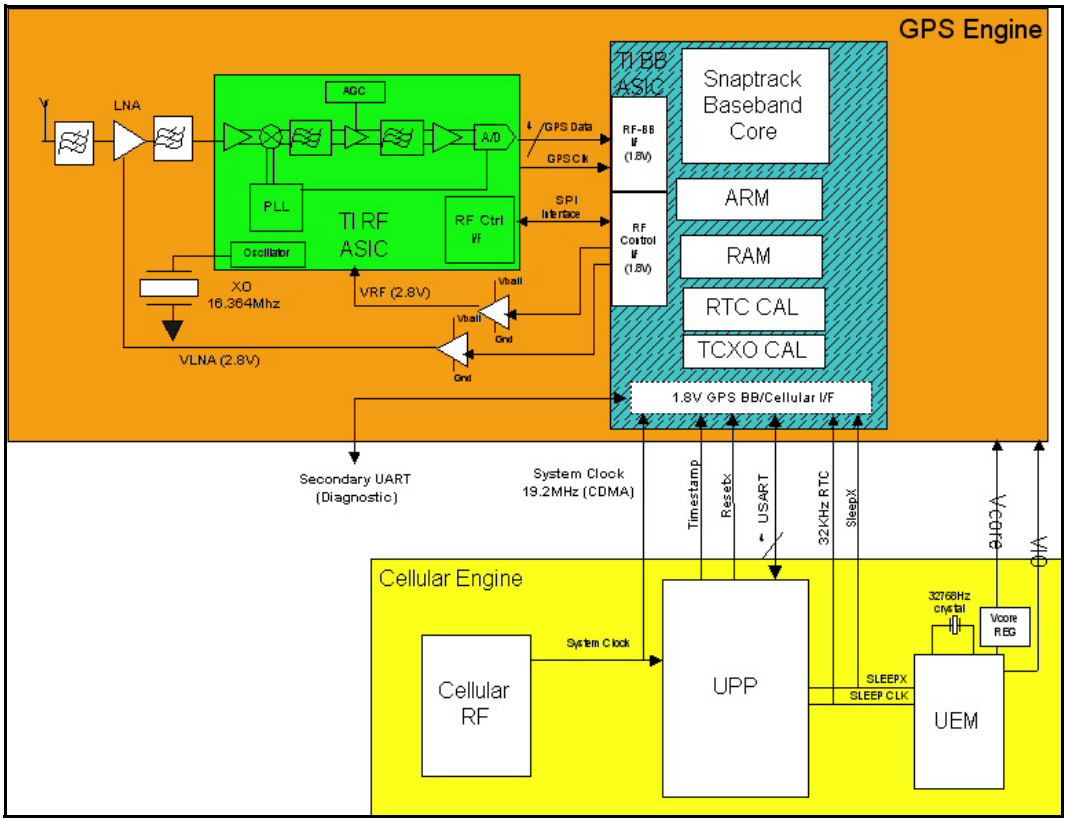


Figure 25: GPS block diagram

The basic GPS BB troubleshooting method is to put the GE and CE in the proper mode, then check to make sure that necessary inputs from the CE are good (power, clock, etc.). Ensure that these inputs produce the proper outputs. Because of the large level of integration (most functionality is contained in the two ASIC chips), the amount of diagnostics one is able to do is limited.

Prior to performing diagnostics, perform a visual inspection on the GPS circuitry to see if the problem is physical (dislodged parts, corrosion, poor solder joints, etc.)

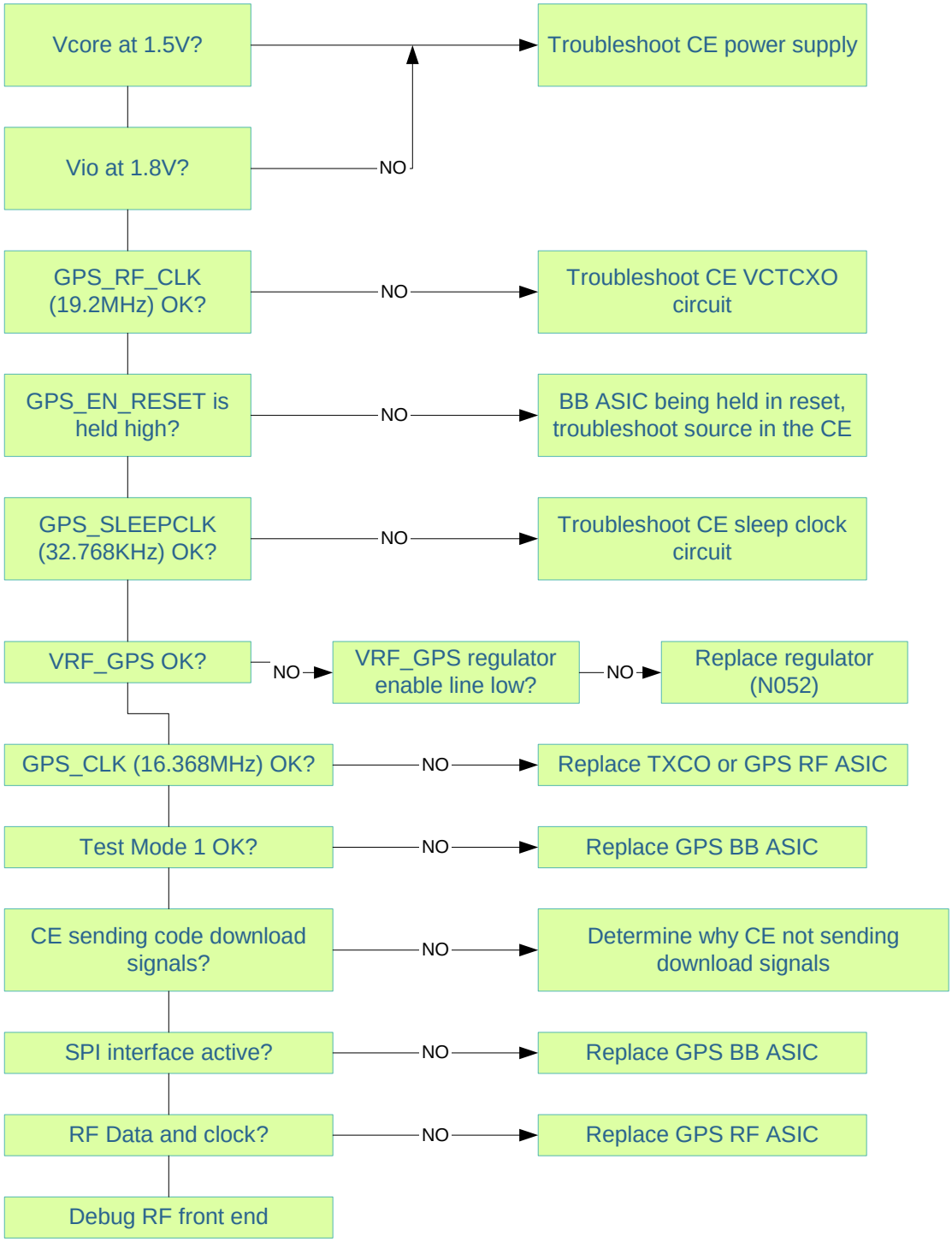


Figure 26: GPS troubleshooting flowchart

This page intentionally left blank.